

Overview of Simulation Strategies for Nanoelectronics

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Outline

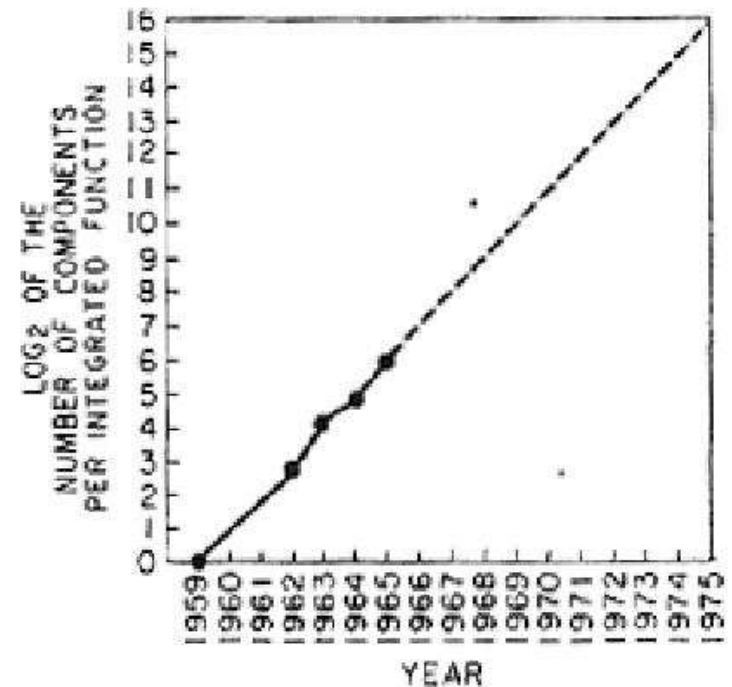
- ⇒ **Introduction to Nanoelectronics**
- ⇒ **Nanoelectronics in ITRS**
- ⇒ **Molecular Simulation**
- ⇒ **Conclusion**

Moore's Law

- ⇒ **Exponential growth.**
- ⇒ **Cost per function reduction:**
 - 25-29% per year.
- ⇒ **Market growth:**
 - On average 17% per year.
- ⇒ **The law holds for about 45 years.**
- ⇒ **ITRS**
 - Industry want to keep with this law further.

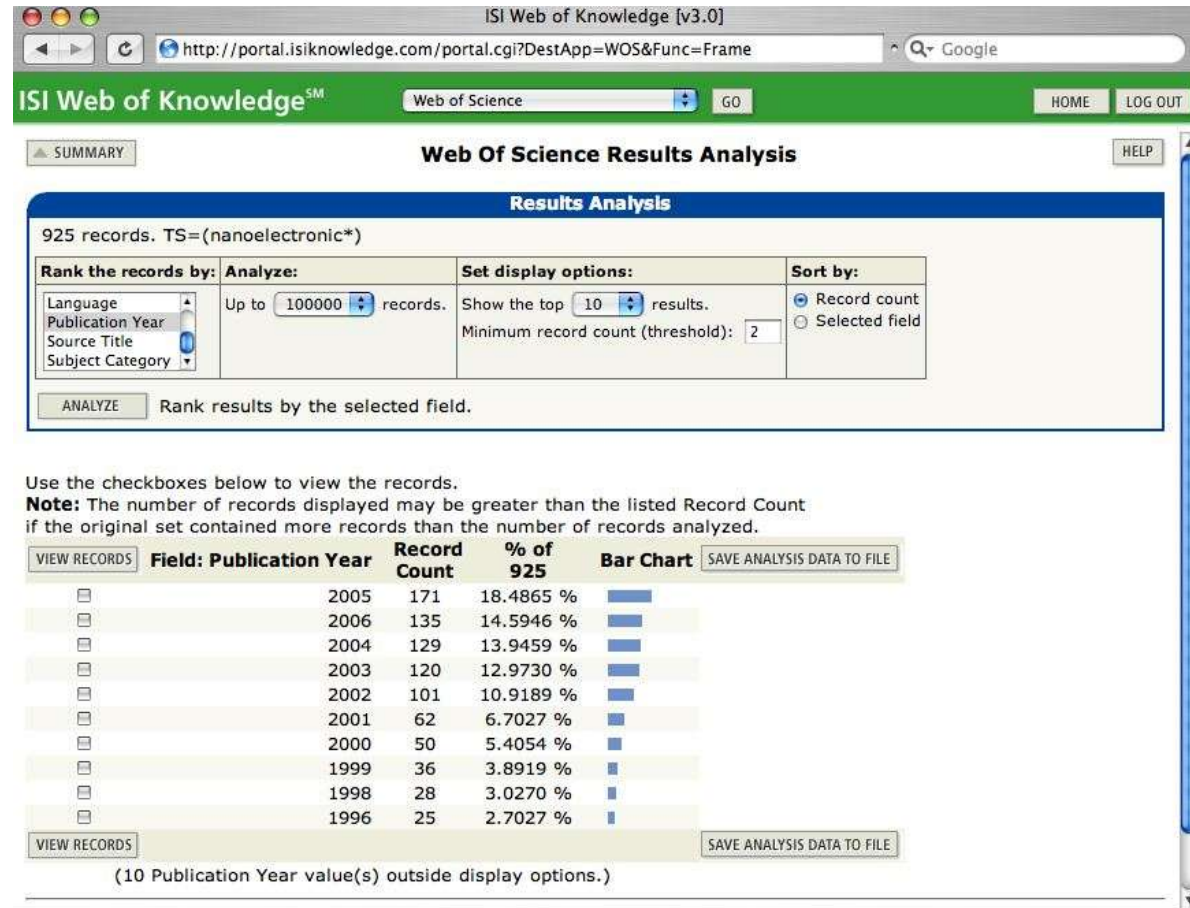
Gordon E. Moore, 1965

Cramming more components
onto integrated circuits



Papers on Nanoelectronics: Web of Science

- ⇒ **925 papers:**
 - Refereed journals.
- ⇒ **Search includes:**
 - Title,
 - Keywords,
 - Abstract.



Papers on Nanoelectronics: IEEE

- ⇒ 1681 papers.
- ⇒ Only IEEE publications.
- ⇒ IEEE conferences are included.

IEEE Xplore# Search Result

http://ieeexplore.ieee.org/search/searchresult.jsp?history=yes&queryText=%28%28nanoelectronic*<in>metadata%29%29

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Search Results

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A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.

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by Luryi, S.; Xu, J.; Zaslavsky, A.;
Hardcover, Edition: 1
View All 1 Result(s)

Key

IEEE JNL	IEEE Journal or Magazine
IEEE JNL	IEEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEEE CNF	IEEE Conference Proceeding
IEEE STD	IEEE Standard

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((nanoelectronic*)<in>metadata)

Check to search only within this results set

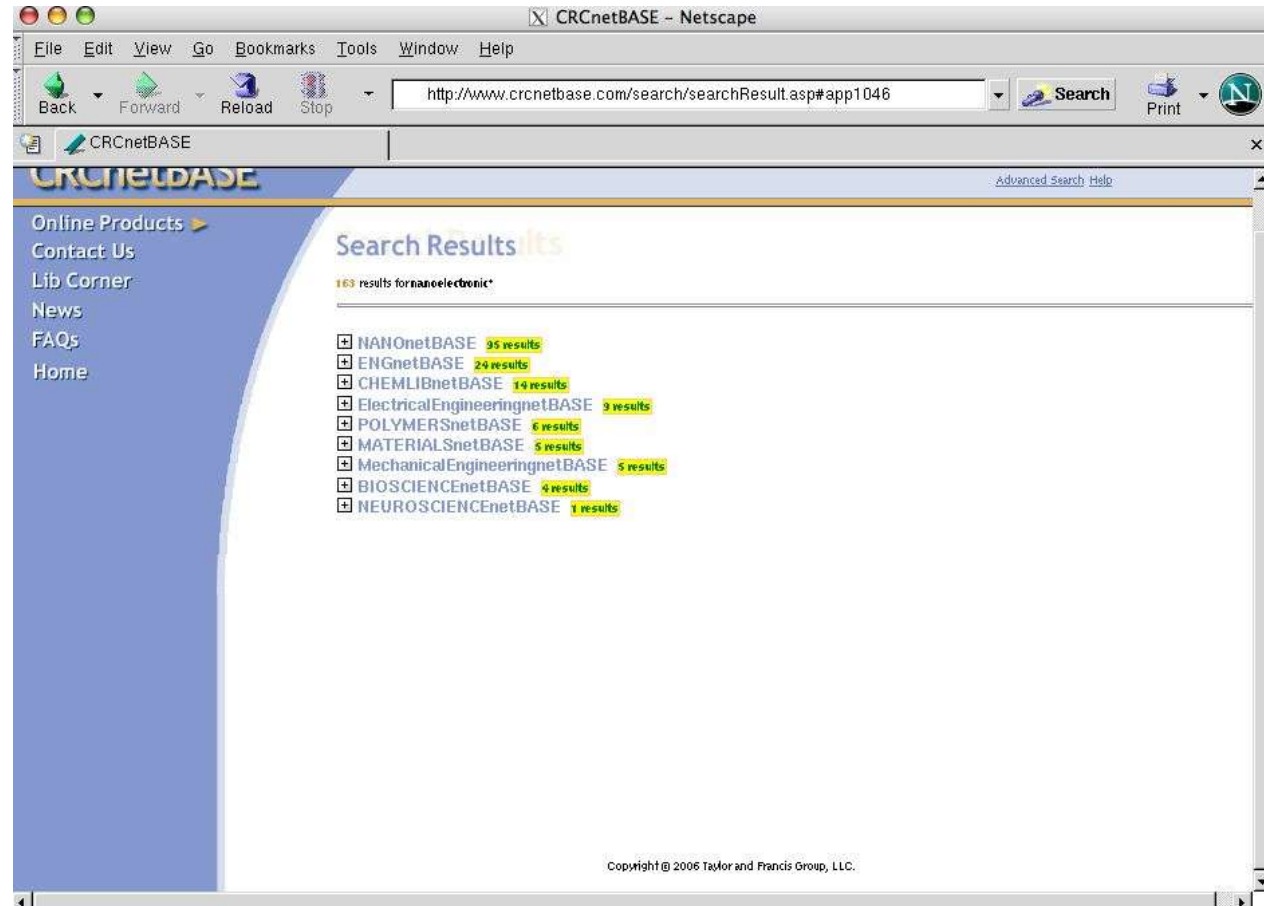
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view selected items Select All Deselect All View: 1-25 | 26-50 | 51-75 | 76-100

1. Special issue on nanoelectronic circuits and nanoarchitectures
Circuits and Systems I: Regular Papers, IEEE Transactions on [see also Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on]
Volume 53, Issue 9, Sept. 2006 Page(s):2096 - 2096
Digital Object Identifier 10.1109/TCSI.2006.884337
AbstractPlus | Full Text: PDF(184 KB) IEEE JNL
Rights and Permissions
2. Special issue on nanoelectronic circuits and nanoarchitectures
Circuits and Systems I: Regular Papers, IEEE Transactions on [see also Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on]
Volume 53, Issue 8, Aug. 2006 Page(s):1856 - 1856
Digital Object Identifier 10.1109/TCSI.2006.882337
AbstractPlus | Full Text: PDF(184 KB) IEEE JNL
Rights and Permissions
3. Subthreshold behavior of dual-bit nonvolatile memories with very small regions of trapped

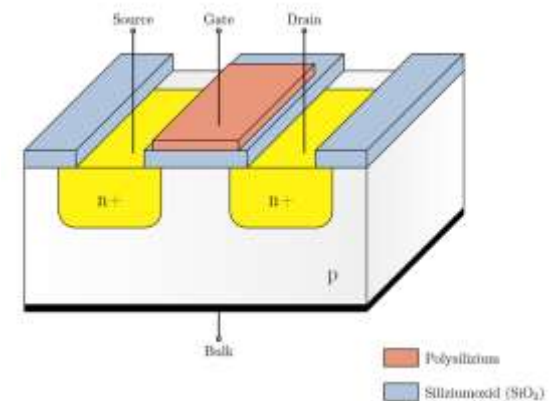
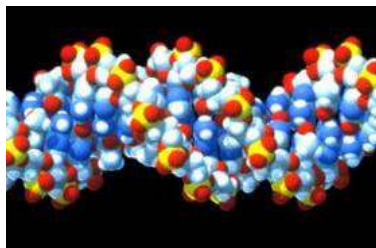
CRC On-Line Book Chapters

⇒ 163 Hits

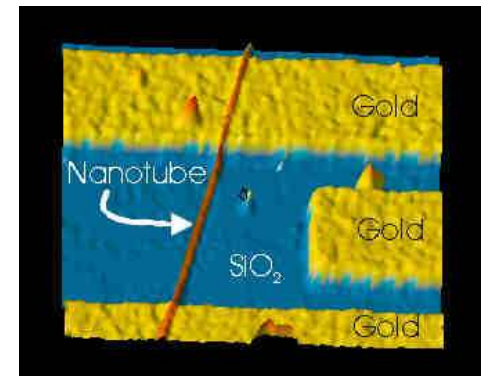


What is Nanoelectronics?

- ⇒ **Electronics on a nanometer scale**
(feature size less than 100 nm)
- ⇒ **Si-based (CMOS) and beyond-CMOS**
- ⇒ **Is “electro” important?**
 - Information processing

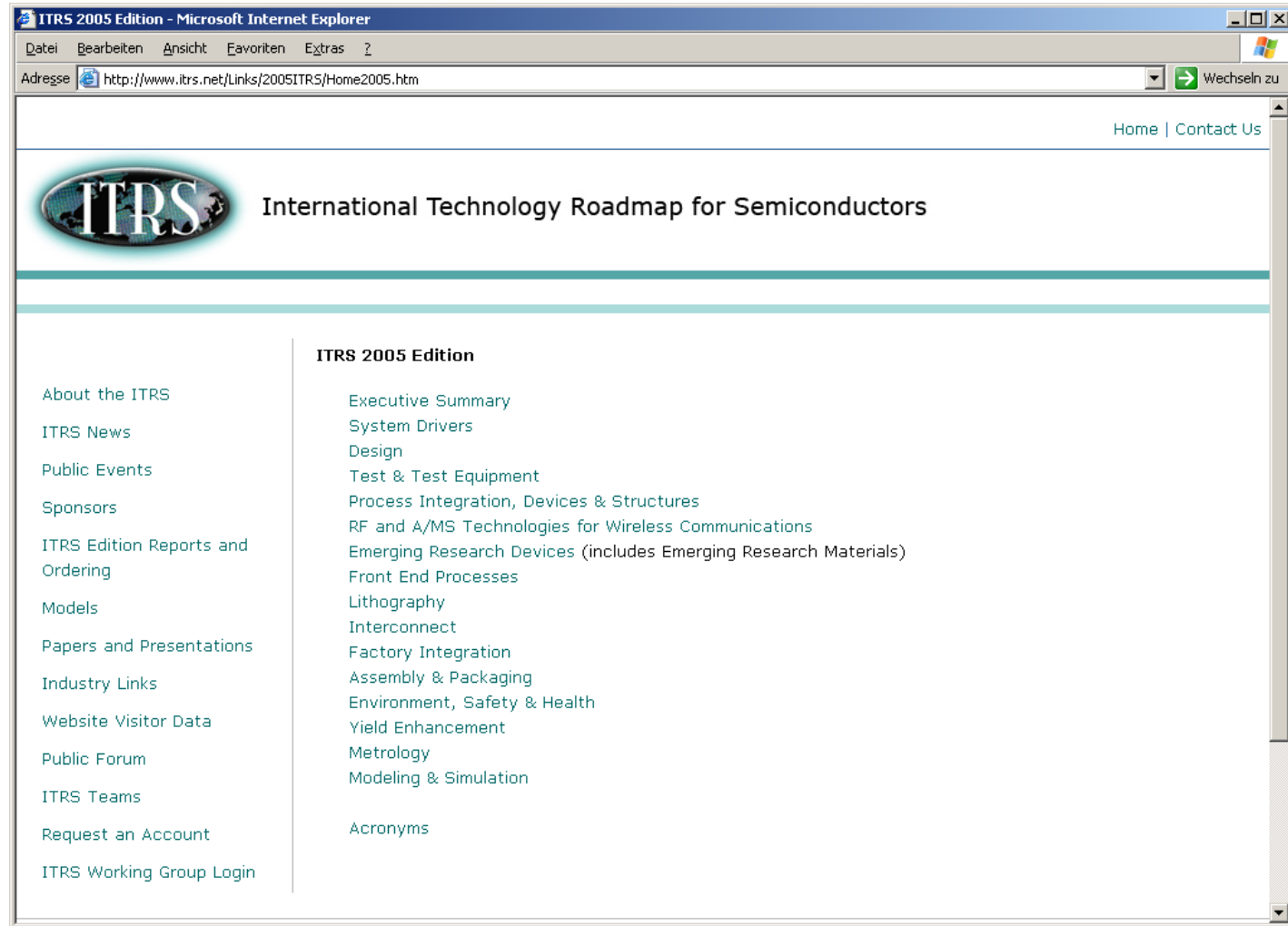


Carbon nanotube transistor



ITRS 2005

What technical capabilities need to be developed for the industry to stay on Moore's Law and the other trends?



Contributors

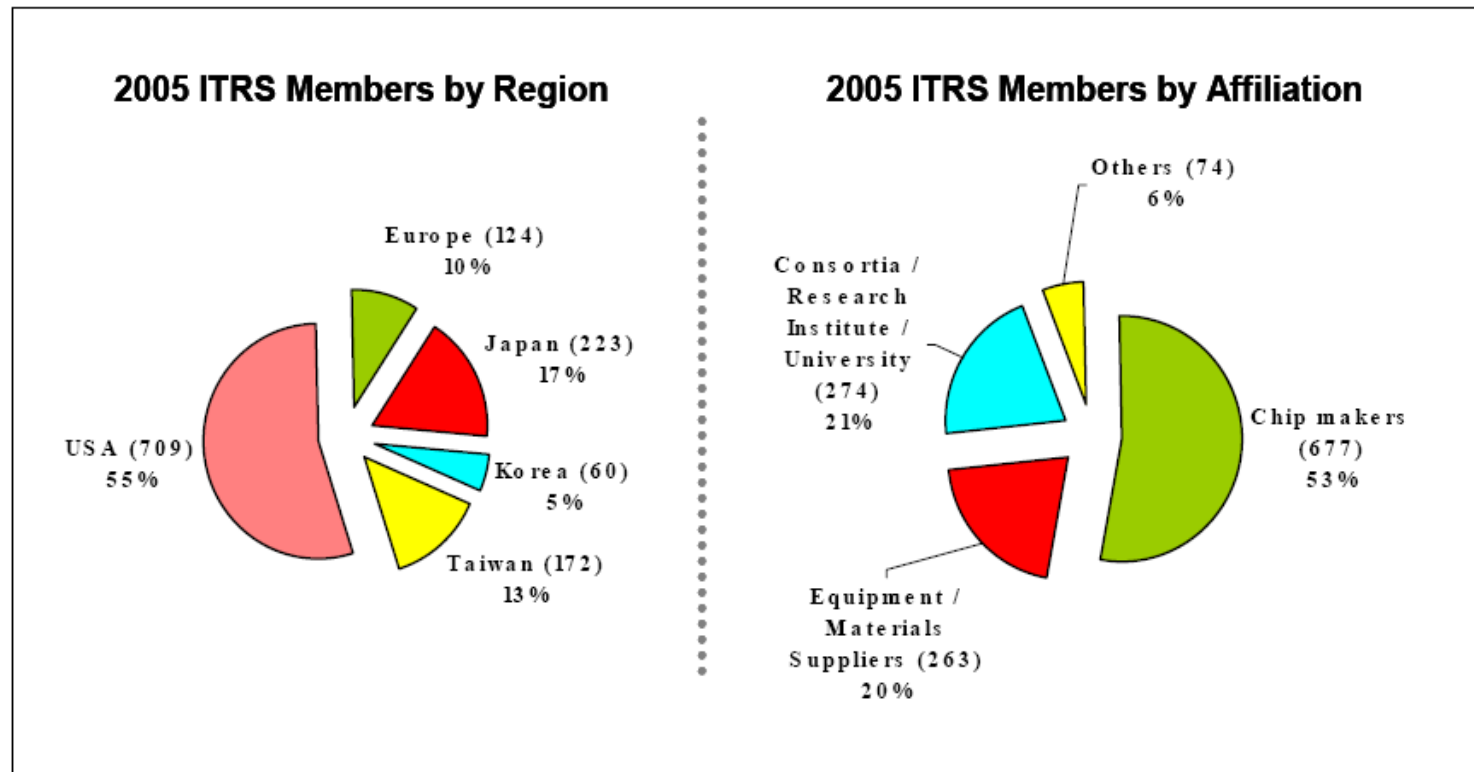
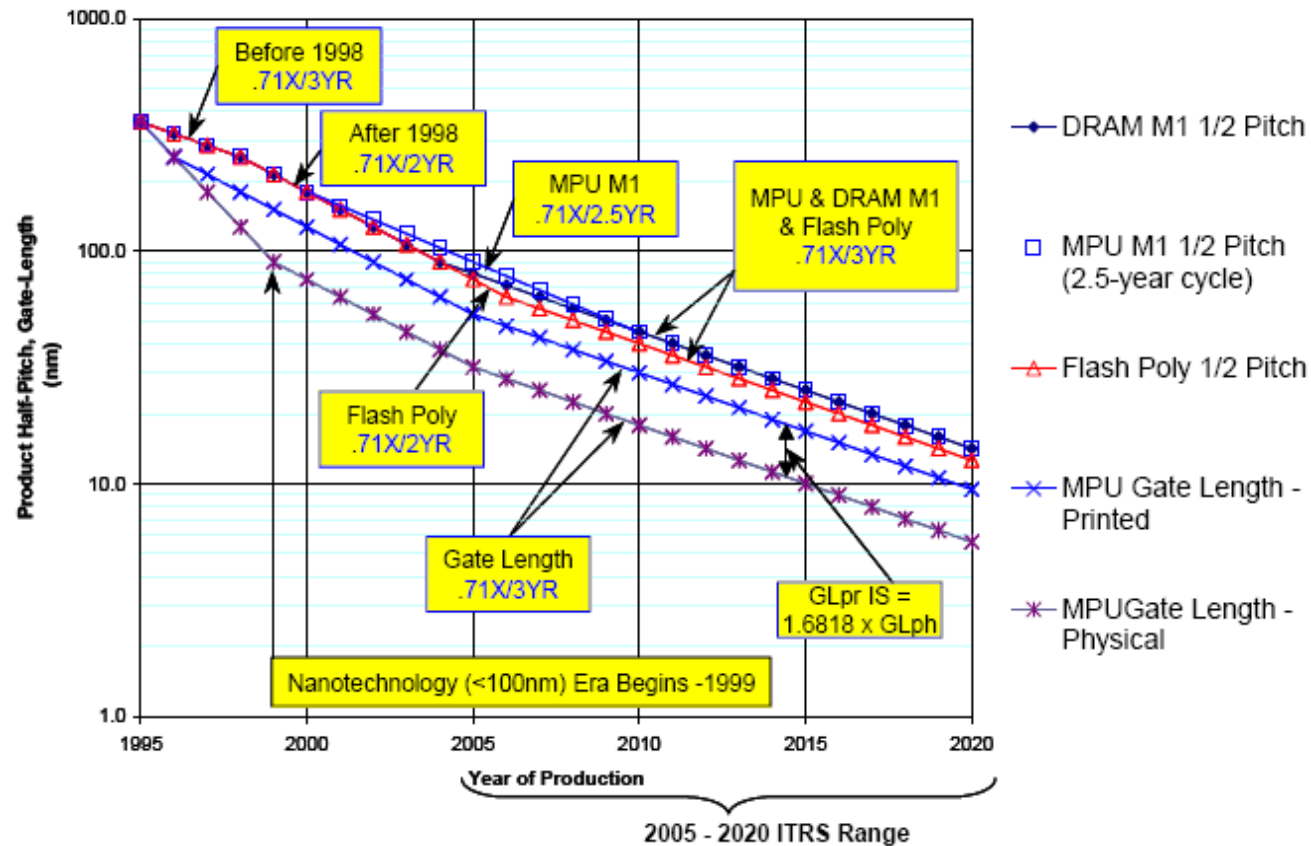


Figure 1 Composition of the ITRS Teams—1288 Global Participants

Structure

- ⇒ **Executive Summary (89 pages)**
- ⇒ **11 Focus International Technology Working Groups**
 - ...
 - Emerging Research Devices / Emerging Research Materials
 - ...
- ⇒ **4 Crosscut International Technology Working Groups**
 - ...
 - Modeling and Simulation

ITRS Product Technology Trend



Near-term
Years:
2005 to 2013

Long-term
Years:
2014 to 2020

Scaling CMOS

Table 76a Lithography Technology Requirements—Near-term Years

Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
DRAM ½ pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
DRAM and Flash									
DRAM ½ pitch (nm)	80	70	65	57	50	45	40	35	32
Flash ½ pitch (nm) (un-contacted poly)	76	64	57	51	45	40	36	32	28
Contact in resist (nm)	94	79	70	63	56	50	44	39	35
Contact after etch (nm)	85	72	64	57	51	45	40	36	32
Overlay [A] (3 sigma) (nm)	15	13	11	10	9	8	7.1	6.4	5.7
CD control (3 sigma) (nm) [B]	8.8	7.4	6.6	5.9	5.3	4.7	4.2	3.7	3.3

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

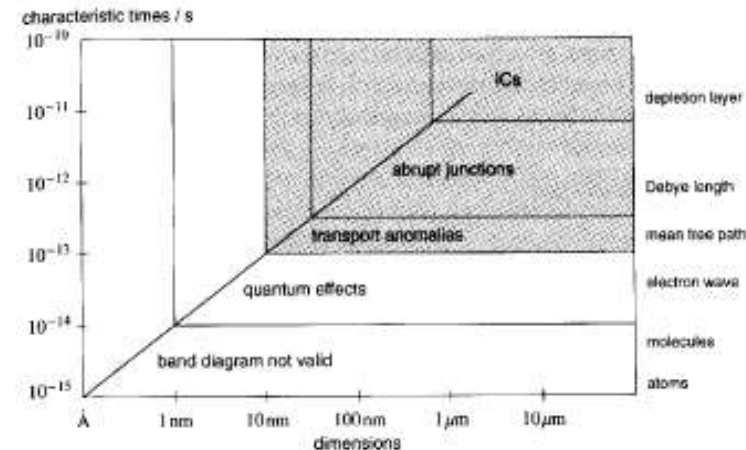
Interim solutions are known

Manufacturable solutions are NOT known



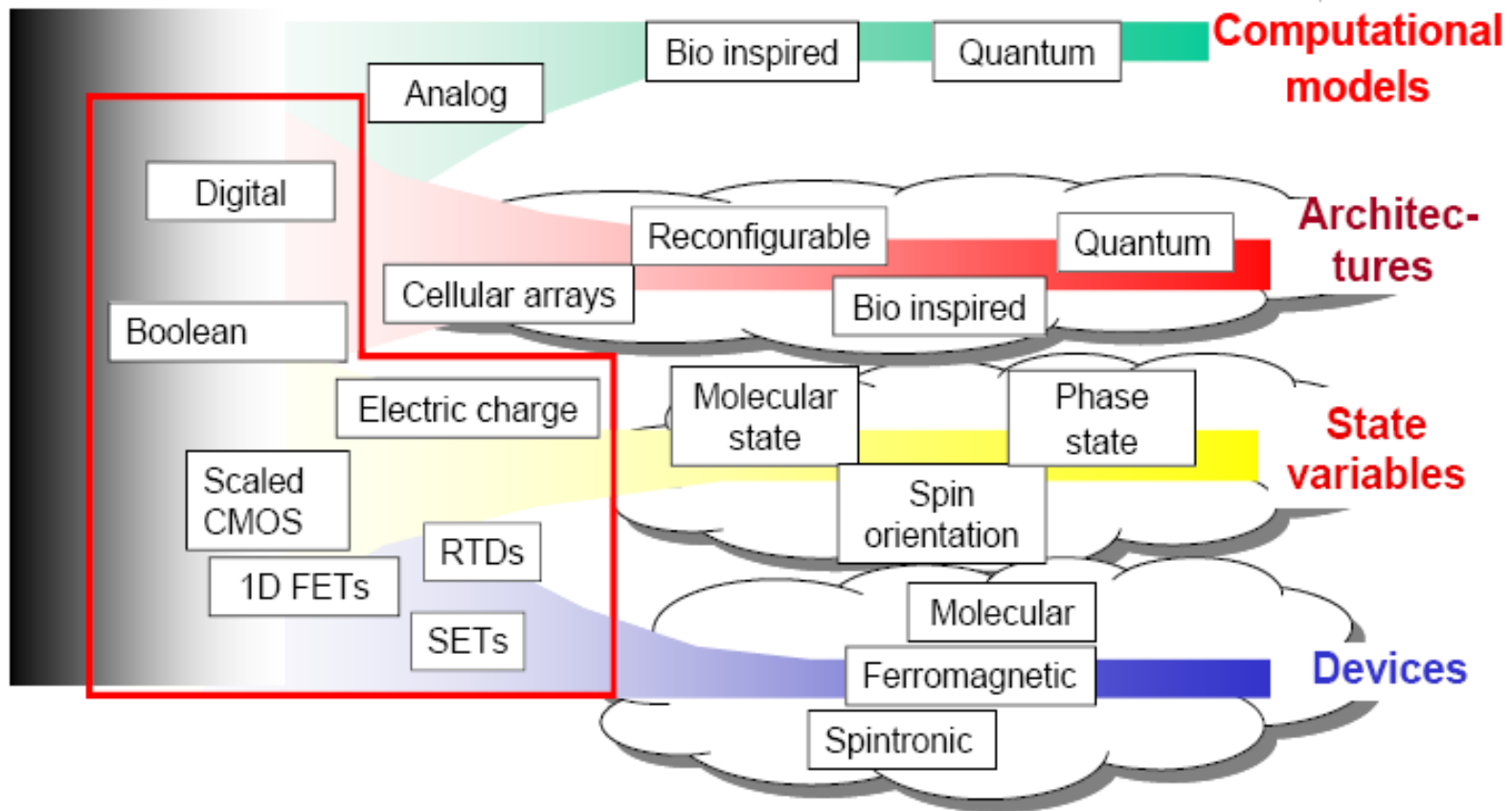
CMOS and beyond CMOS

- ⇒ CMOS is the workhorse of the industry.
- ⇒ Yet, scaling of CMOS has technological and physical limits.
- ⇒ **The semiconductor industry's future success continues to depend on new ideas.**
- ⇒ Chapter on Emerging Research Devices including Emerging Research Materials.



Goser Gloeserkoetter Dienststuhl

Taxonomy for Nano Information Processing



Devices and Architectures

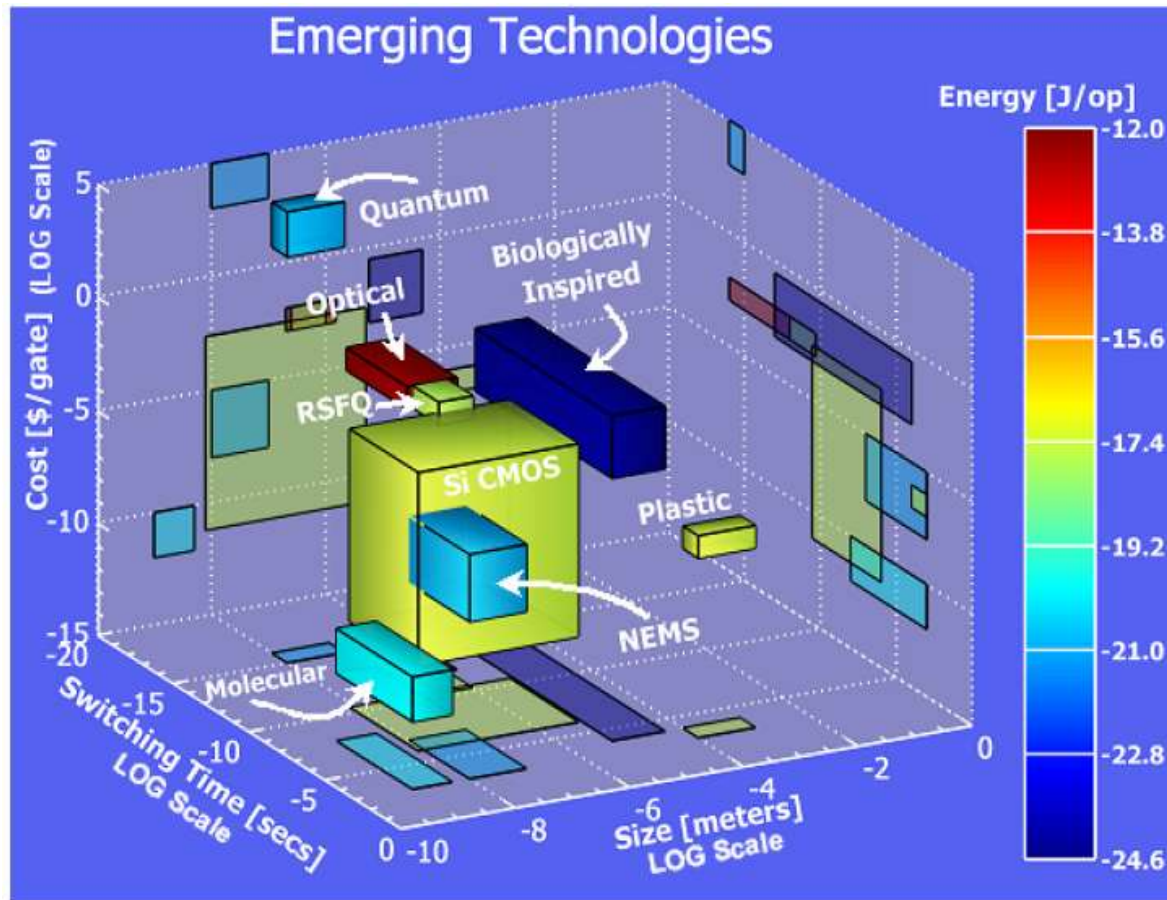
⇒ **Devices:**

- Carbon nanotube and nanowires,
- Ferroelectric FET memory,
- Molecular,
- Nano floating gate memory,
- Polymer memory,
- Polymer transistor,
- Resonant tunneling devices,
- Spin transistor.

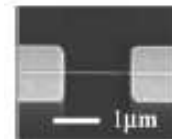
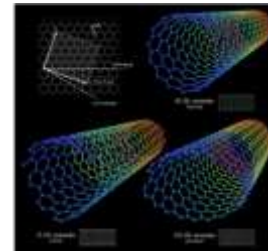
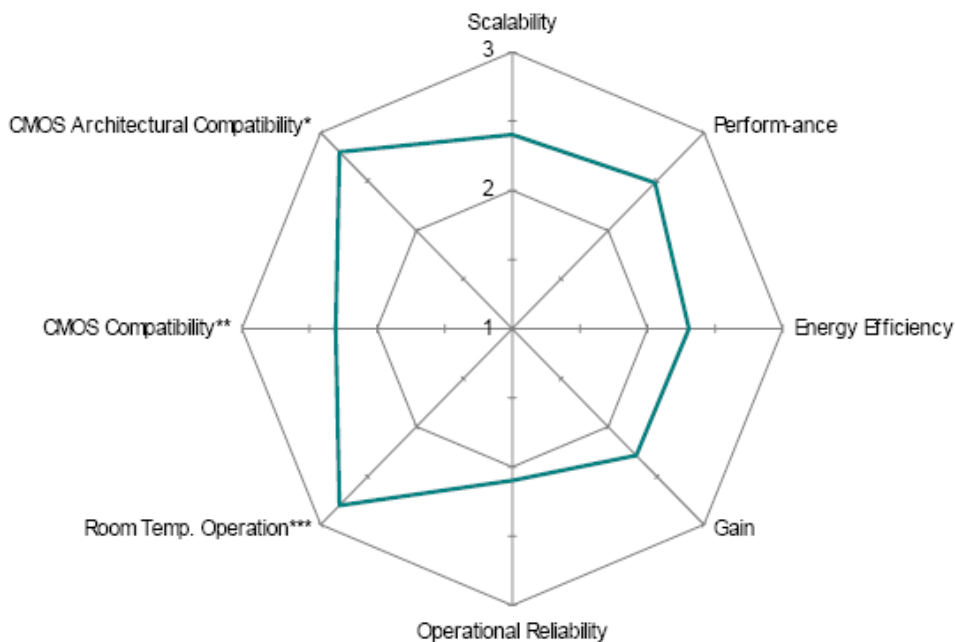
⇒ **Architectures:**

- Quantum Cellular Automata,
- Cellular Nonlinear Networks,
- Reconfigurable Implementations,
- Biologically Inspired Implementation.

Emerging Technologies and CMOS



Potential Solutions for Logic Devices (CNT and NW)

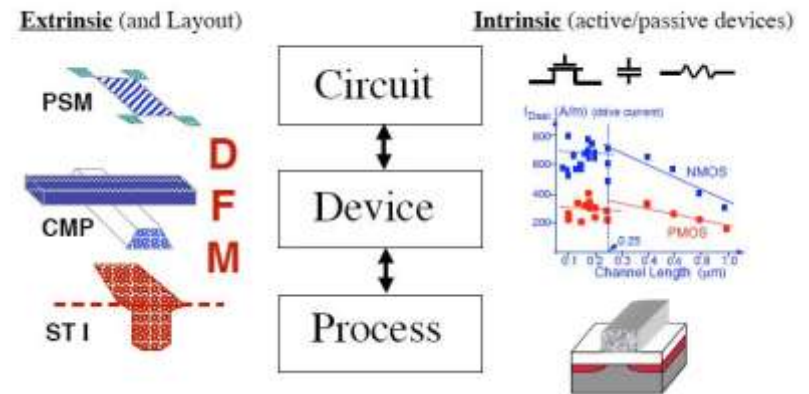


NW-FET

3	<p>Substantially exceeds CMOS</p> <p>* <i>or</i> is compatible with CMOS architecture</p> <p>** <i>or</i> is monolithically integrable with CMOS wafer technology</p> <p>***<i>or</i> is compatible with CMOS operating temperature (i.e., Substantially Better than Silicon Logic)</p>
2	<p>Comparable to CMOS</p> <p>* <i>or</i> can be integrated with CMOS architecture with some difficulty</p> <p>** <i>or</i> is functionally integrable (easily) with CMOS wafer technology</p> <p>***<i>or</i> requires a modest cooling technology, $T \geq 77K$ (i.e., Comparable to Silicon Logic)</p>
1	<p>Substantially (2×) inferior to CMOS</p> <p>* <i>or</i> can not be integrated with CMOS architecture</p> <p>** <i>or</i> is not integrable with CMOS wafer technology</p> <p>***<i>or</i> requires very aggressive cooling technology, $T < 77K$ (i.e., Substantially Worse than Silicon Logic)</p>

Modeling and Simulation: Technology CAD for CMOS

- ⇒ High-frequency device and circuit modeling
- ⇒ Front-end process modeling
- ⇒ Integrated modeling of equipment and materials
- ⇒ Lithography simulation
- ⇒ Thermo-mechanical-electrical modeling for interconnections and packages



Modeling and Simulation: Molecular Simulation

- ⇒ **Ultimate nanoscale CMOS simulation**
- ⇒ **Nano-scale modeling of novel devices**
- ⇒ **Modeling of new materials**

- ⇒ **Nanoscale simulation capability including accurate atomistic and quantum effects**

- ⇒ **Algorithms:**
 - Efficient atomistic/quantum models; ab-initio or molecular dynamics based topography simulations;
 - Multi-scale simulation (atomistic-continuum); fast coupling of equipment-topography-electrical-reliability models; hierarchical full-chip simulation.

Model Order Reduction for EDA

⇒ Current EU projects:

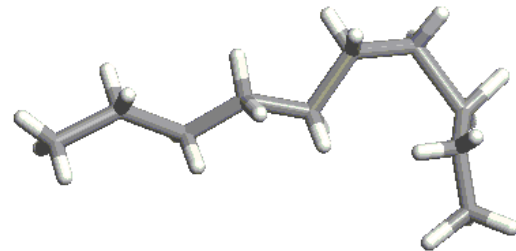
- COMSON (**CO**upled **M**ultiscale **S**imulation and **O**ptimization in **N**anoelectronics)
<http://www.comson.org/>
- CHAMELEON RF, (**C**omprehensive **H**igh-**A**ccuracy **M**odelling of **E**lectromagnetic **E**ffects in **C**omplete **N**anoscale **RF** blocks)
<http://www.chameleon-rf.org/>



- O-MOORE-NICE, (**O**perational **M**odel **O**der **R**eduction for **N**anoscale **IC** **E**lectronics)

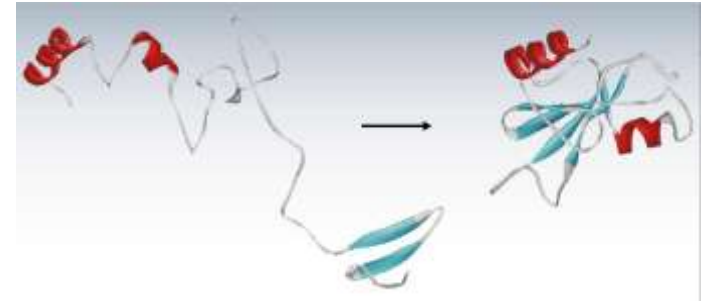
Course: Molecular Simulation for MST

- ⇒ **J. G. Korvink, E. B. Rudnyi**
 - <http://evgenii.rudnyi.ru/teaching.html#md>
- ⇒ **Introductory course for MST engir**
- ⇒ **12 lectures, 3 computational labs**



From the First Principles

- ⇒ **Ab initio (*from the beginning*)**
- ⇒ **Input: A few fundamental constants**
 - electron mass, proton mass, Plank constant, speed of light, ...
- ⇒ **Output: Everything**
- ⇒ **Computationally expensive**
- ⇒ **Blue Gene: IBM Petaflop computer**
 - Protein folding

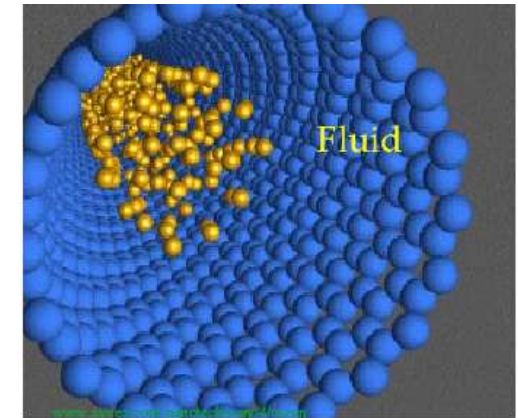
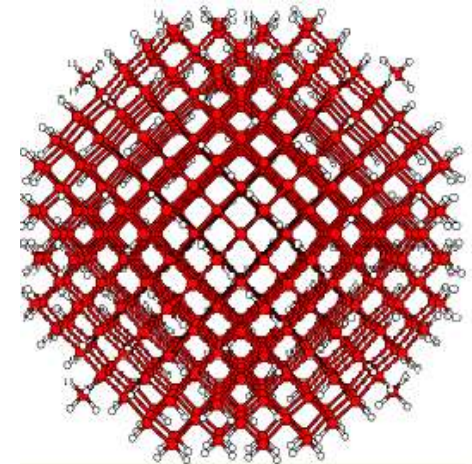


Hierarchy

- ⇒ **Potential Energy Surface (0 K)**
 - Electronic Schrödinger Equation
 - Semiempirical methods
 - Molecular Mechanics

- ⇒ **Adding Entropy and Temperature**
 - Molecular Dynamics
 - Monte Carlo

- ⇒ **QSAR (empirical correlations)**



Schrödinger Equation

Nuclei (R) and electrons (r) :

$$\Psi(R, r)$$

$$H\Psi = E\Psi$$

$$H = T_{\text{nuc}} + T_{\text{elec}} + U_{\text{nuc-nuc}} + U_{\text{elec-electc}} + U_{\text{elec-nuc}}$$

$$H = \sum_n \frac{-\hbar^2}{2m_n} \nabla_n^2 + \sum_i \frac{-\hbar^2}{2m_e} \nabla_i^2 + \sum_{\text{Pairs of Nuclei}} \frac{Z_n Z_m e^2}{r_{nm}} + \sum_{\text{Pairs of Elec.}} \frac{e^2}{r_{ij}} - \sum_{n,i} \frac{Z_n e^2}{r_{in}}$$

del operator for nuclei

del operator for electron

mass of nucleus

mass of electron

at. # of n^{th} nucleus

distance between nuclei n and m

distance between electrons i & j

distance between electron i & nucleus n

Potential Energy Surface

⇒ **Born-Oppenheimer Approximation**

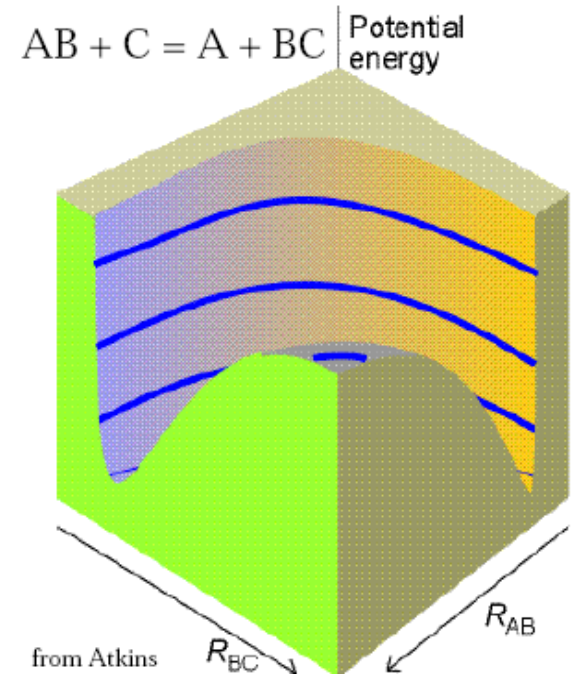
⇒ Proton is 1836 times heavier than electron.

→ **Factorize for nuclei part**

$$\Psi(R, r) = \Psi(R)\psi(r;R)$$

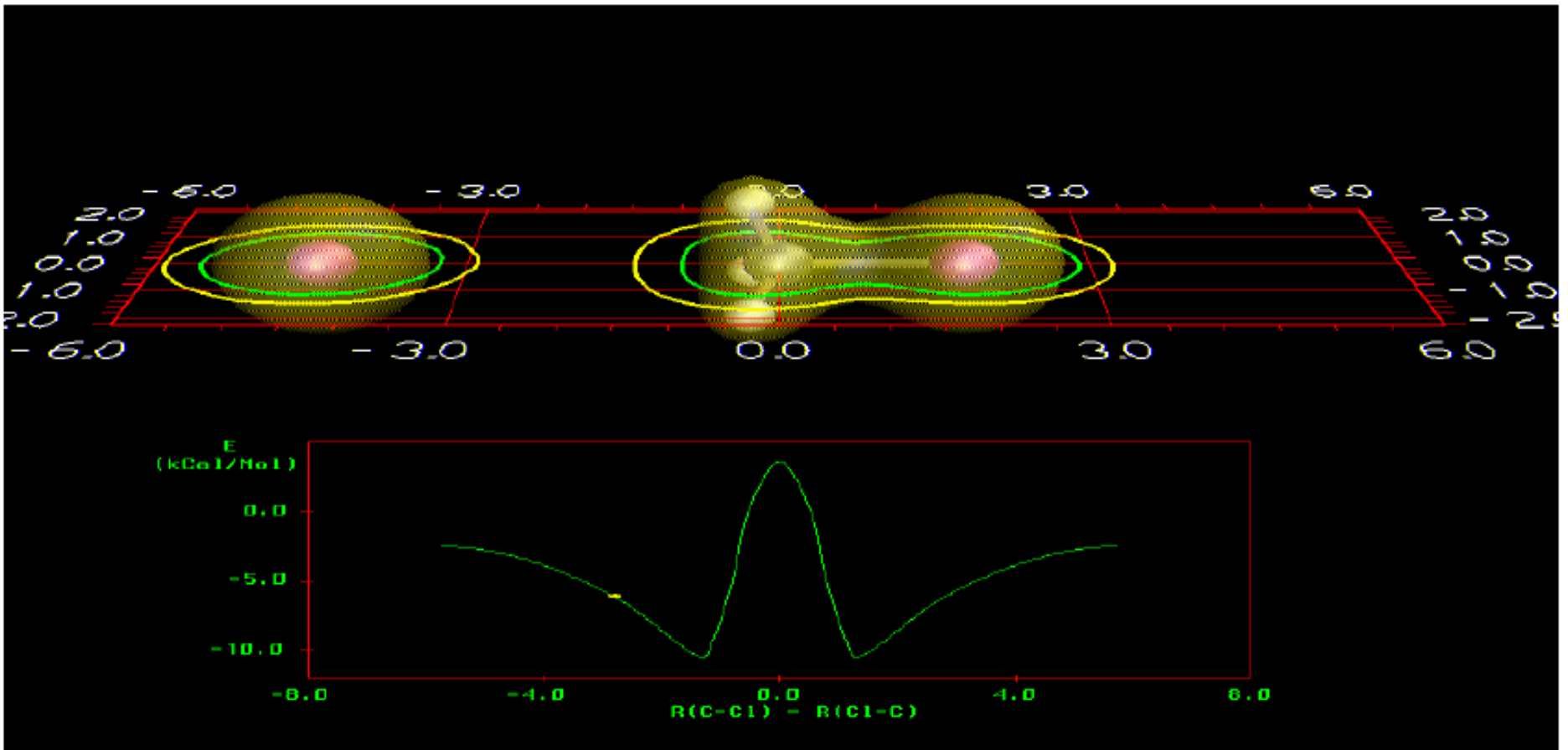
→ **Schrödinger equation for electrons**

$$H_{el}\psi(r;R) = E_{el}(R)\psi(r;R)$$

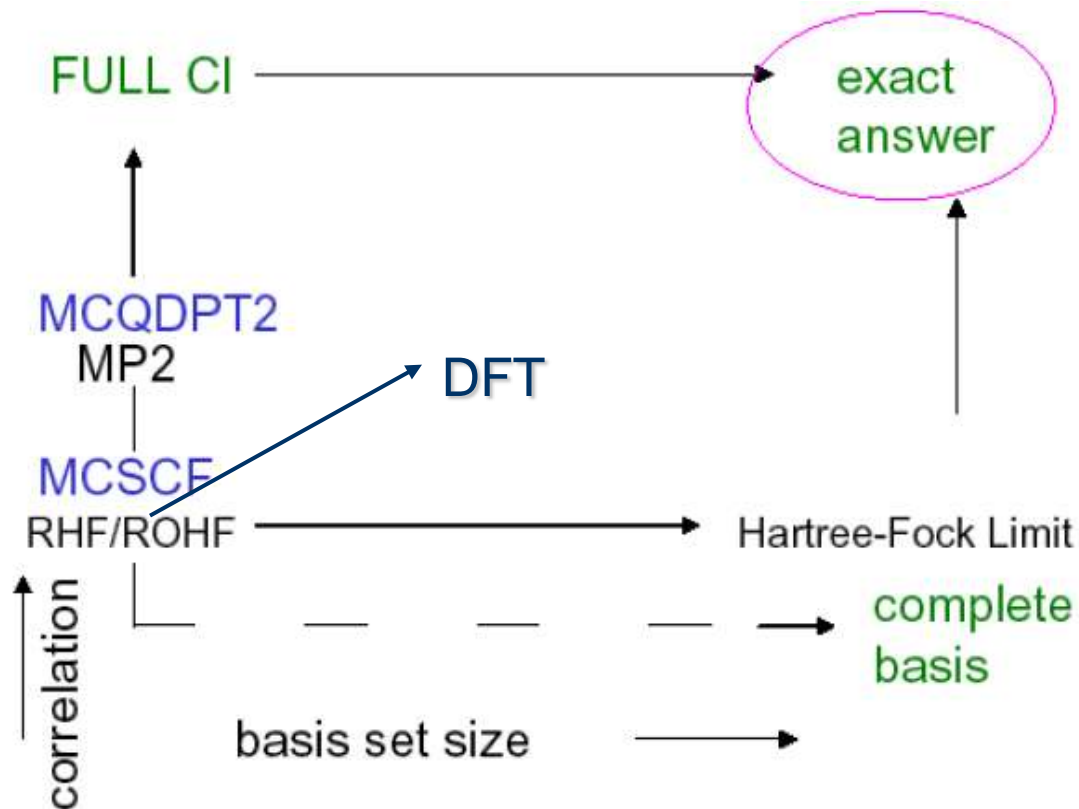


PES Example

scsg9.unige.ch/fln/eng/toc.html



Quantum Chemistry Methods



Molecular orbitals

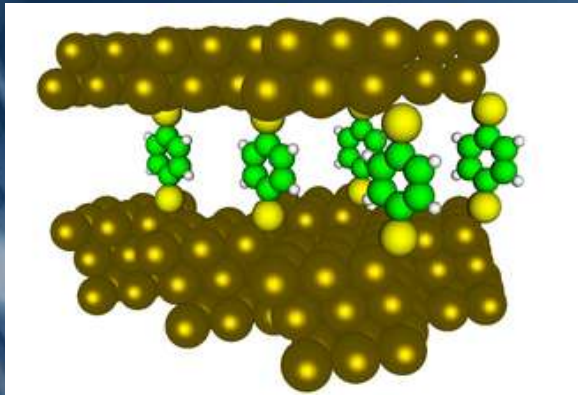
$$\Psi(1,2,\dots,N) \approx \psi(1)\psi(2)\dots\psi(N)$$

Atomic orbitals

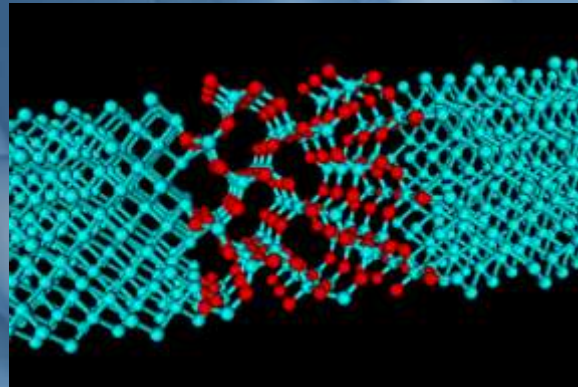
$$\psi = \sum_i c_i \vartheta_i$$

What kind of software is needed?

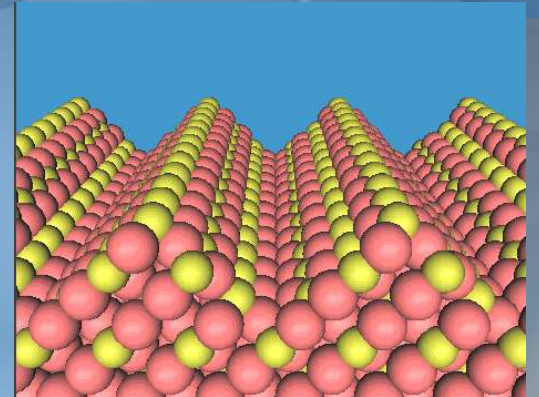
As the main challenge in nanoscale technology derive from quantum phenomena across nanoscale junctions, interfaces and surfaces, it is critical to be able to accurately model such phenomena from quantum theory



Junctions



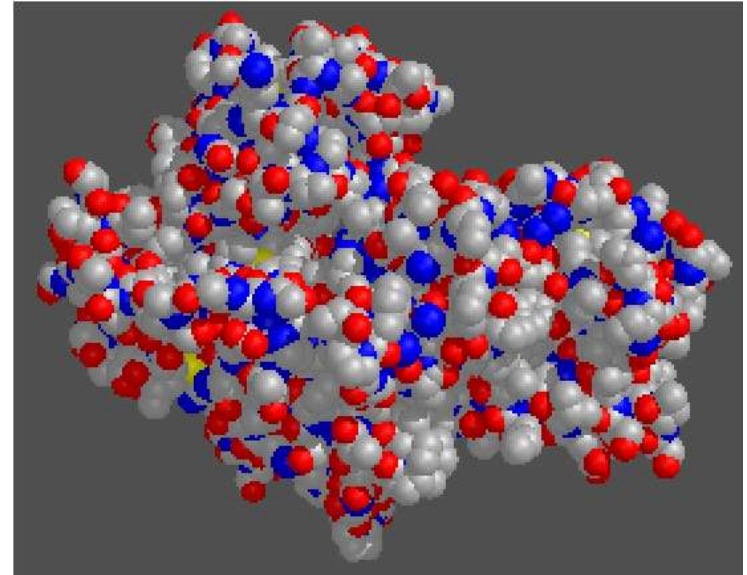
Interfaces



Surfaces

Semiempirical Methods

- ⇒ Consider valence electrons only
- ⇒ Neglect some integrals
- ⇒ Parameterize the others
- ⇒ Accuracy depends on the parameterization

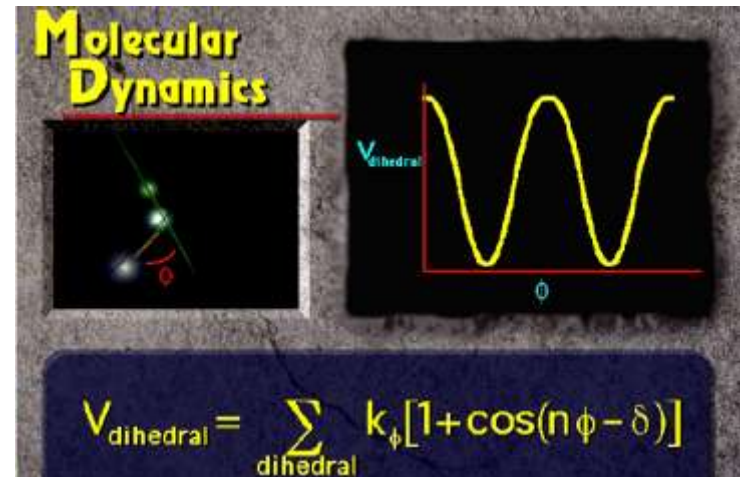
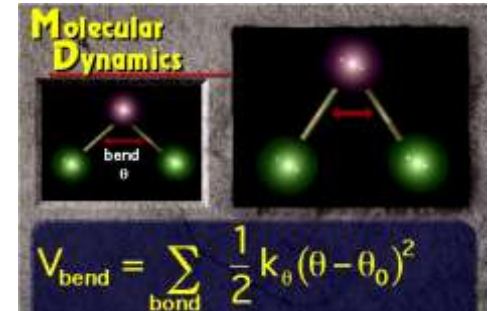
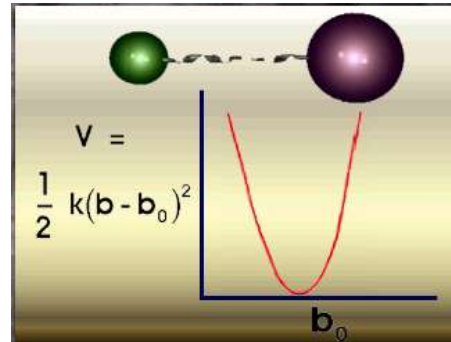


Molecular Mechanics

⇒ Empirical force field

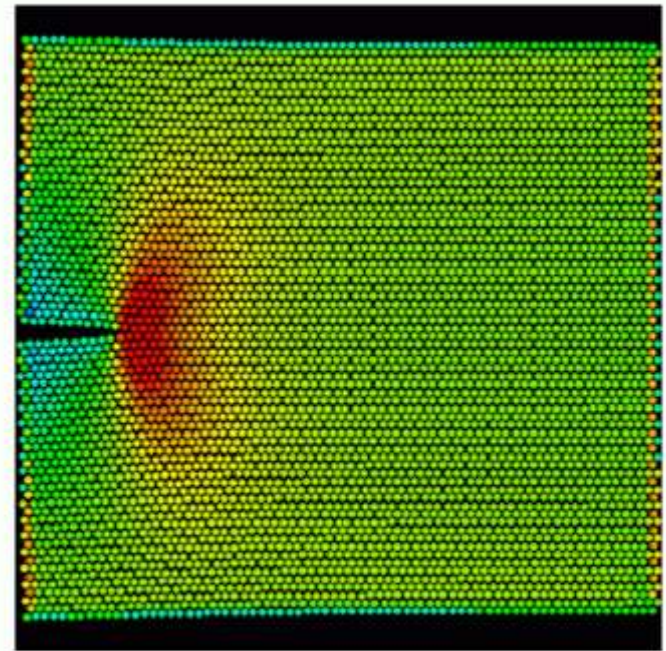
- Bonding: stretching, bending, torsion, cross-terms;
- Not-bonding: van der Waals, electrostatic, hydrogen, etc...

⇒ Accuracy depends on the force field employed

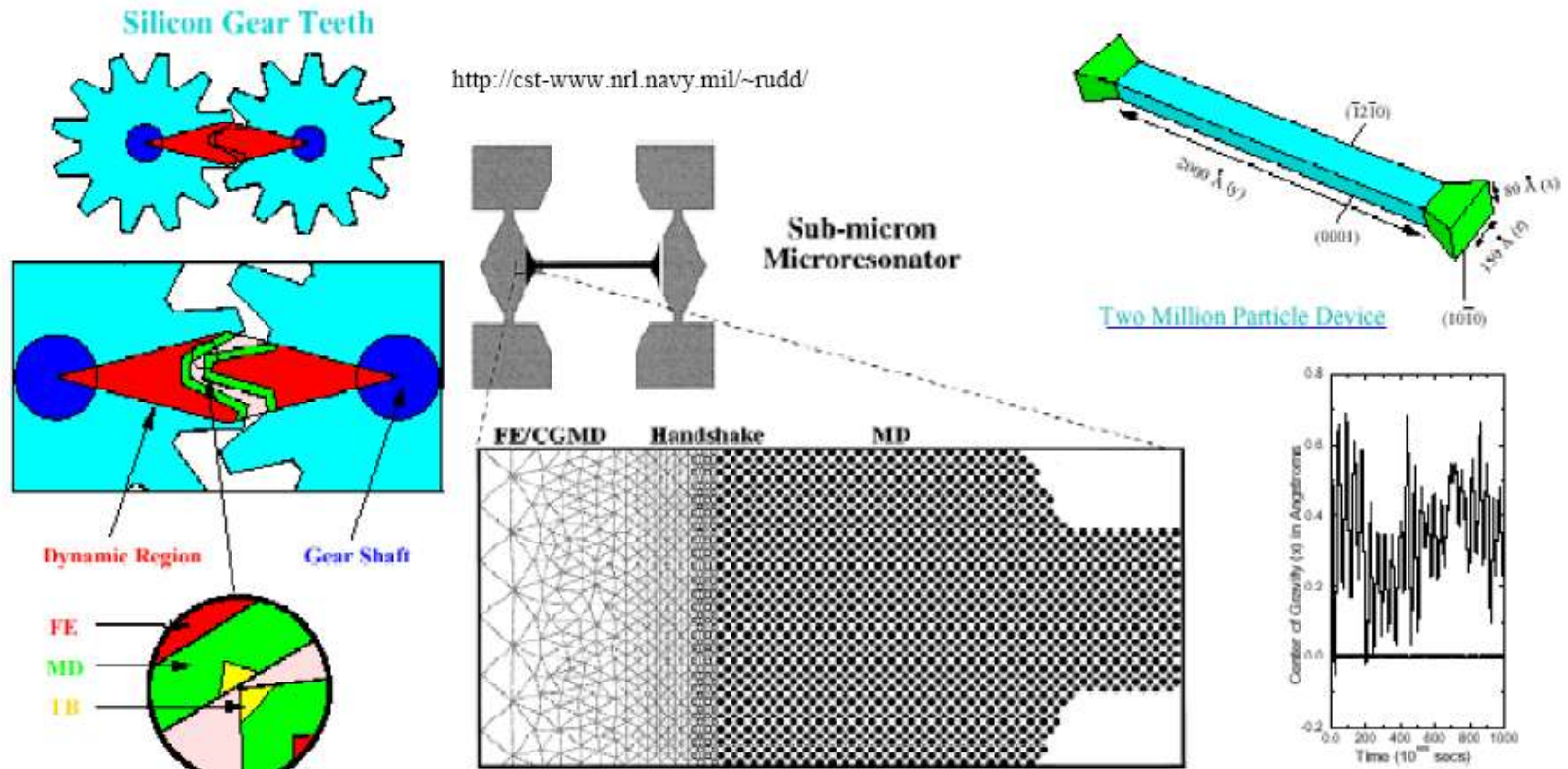


Molecular Dynamics and Monte Carlo

- ⇒ **Input:**
 - Potential energy surface
- ⇒ **Output:**
 - Heat conductivity, viscosity, ...
- ⇒ **Time average**
 - Integrating in time
- ⇒ **Ensemble average**
 - Sampling according to Boltzmann distribution

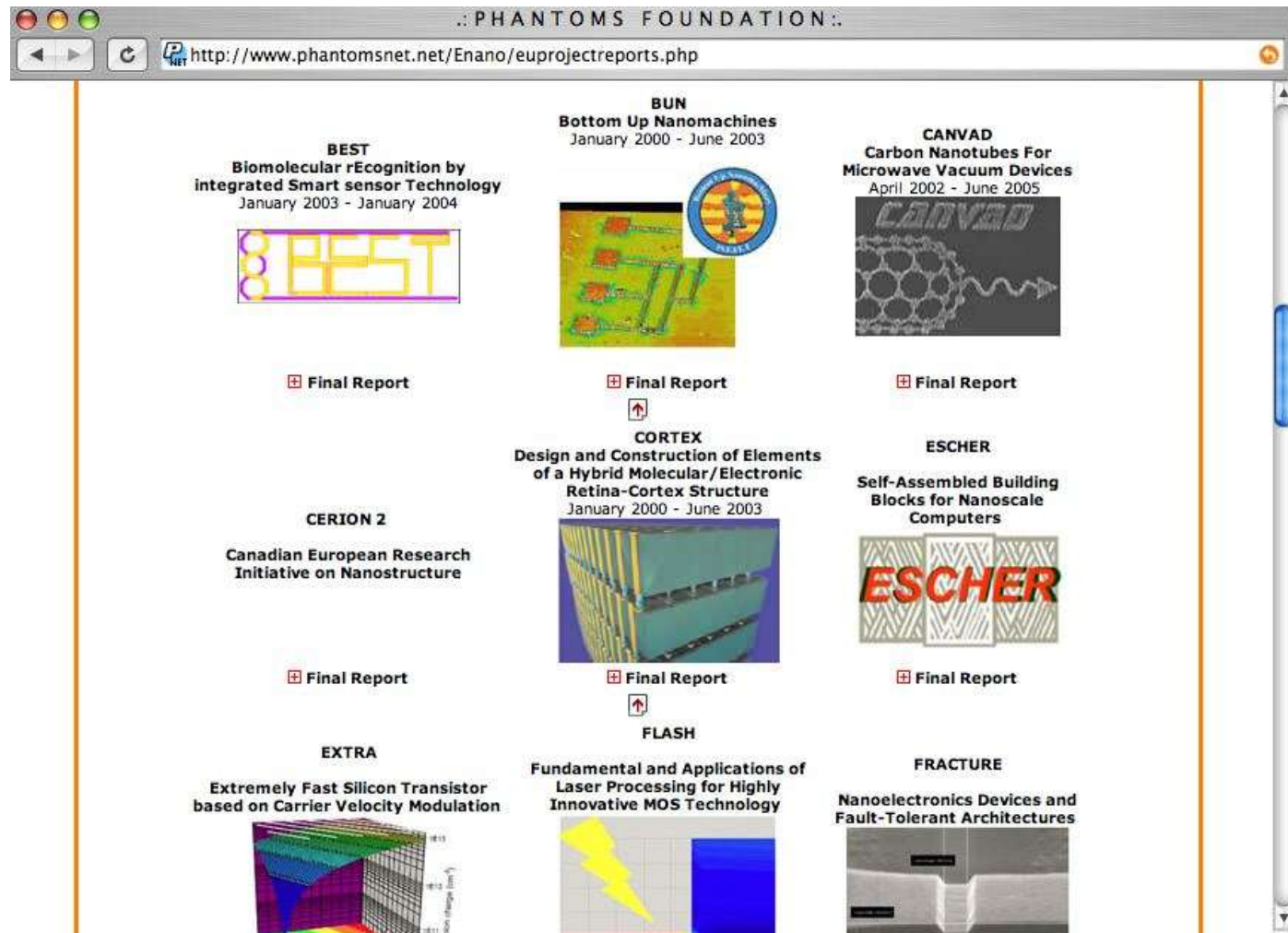


Multiscale Simulation



Conclusion

- ⇒ **Beyond CMOS: New ideas for nanoelectronics**
- ⇒ **Molecular simulation is a natural way to check new ideas**
- ⇒ **Tight collaboration between industry and academia**





ISTweb - ENIAC - Home page

http://cordis.europa.eu/ist/eniac/home.html

CORDIS / ISTweb / ENIAC / Home page

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European Nanoelectronics Initiative Advisory Council

Securing global leadership, creating competitive products, sustaining high innovation and top-class skills.

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ENIAC is the European Technology Platform for Nanoelectronics

The principal mission of ENIAC is to:

- Provide a strategic research agenda for the nanoelectronics sector, with respect to R&D
- Set out strategies and roadmaps to achieve this vision through the Strategic Research Agenda and other associated documents;
- Stimulate increased and more effective and coherent public and private investment in R&D in the nanoelectronics sector;
- Contribute to improving convergence between EC, national, regional and private R&D actions on nanoelectronics within the European Research Area Framework;
- Enhance networking and clustering of the R&D capacity in Europe;
- Promote European commitment to R&D thus ensuring Europe as an attractive location for researchers;
- Interact with other policies and actors at all levels that influence the competitiveness of the sector such as education and training, competition, IPR, finance and investment, etc.

How to express your interest

You are invited to submit an Expression of Interest that should include a short overview of the organisation's activities in the nanoelectronics sector as well as the motivation for participating in ENIAC. A short CV of the person from the organisation that would be the contact point (including a web link) should also be included.

ENIAC Highlights

- ENIAC Strategic Research Agenda (full version) (PDF)
- Forum of Stakeholders 23 November 2005
- Forum of Stakeholders - How to express interest (PDF)
- First meeting of ENIAC Forum of Stakeholders
- Strategic Research Agenda - presentation (PDF)
- Strategic Research Agenda - executive summary (PDF)
- 21 December 2004 - the first meeting of the Steering Committee
- The 2020 Vision document (PDF)
- Nanoelectronics Technology Platform - overview document (PDF)

BMBF: Nanotechnologie – eine Zukunftstechnologie mit Visionen

http://www.bmbf.de/de/nanotechnologie.php

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Bundesministerium für Bildung und Forschung

Ideen zünden!

HIGHTECH-STRATEGIE

BILDUNG

→ **FORSCHUNG**

- ▢ **Neue Technologien**
 - Elektronik und Elektroniksysteme
 - Informationsgesellschaft
 - Mikrosystemtechnik
- **Nanotechnologie**
 - NanoforLife
 - NanoLux
 - NanoMobil
 - Nanobiotechnologie
 - Nanomaterialien
 - Optische Technologien
 - Produktionsforschung
 - Werkstoffforschung
 - Sicherheitsforschung
 - Lebenswissenschaften
 - Grundlagenforschung
 - Umwelt und Nachhaltigkeit
 - Fachhochschulen
 - Sozial- und

HIGHTECH-STRATEGIE

→ **Nanotechnologie - eine Zukunftstechnologie mit Visionen**

Nanotechnologie gilt zunehmend als Zukunftstechnologie schlechthin. Statt "immer höher, immer weiter" lautet ihr Motto "immer kleiner, immer schneller". Die Nanotechnologie erschließt uns die Welt der aller kleinsten Dinge. Ein Nanometer ist der millionstel Teil eines Millimeters. Der Durchmesser eines menschlichen Haares ist fünfzigtausend mal größer. Die Anwendungsmöglichkeiten dieser Technologie sind immens. Die künftigen Fortschritte der Nanotechnologie entscheiden mit über die weitere Entwicklung zukunfts-trächtiger Branchen. Das Bundesforschungsministerium hat hierzu eine Gesamtstrategie vorgestellt.

English version

NANODE 2006

nanoDE 2006 - Strategien für Produkte von morgen
Dritte BMBF-Nanotechnologietage am 6. und 7.11.2006 im Berliner Congress Center.

Die nanoDE richtet sich an Repräsentanten aus Unternehmen im Bereich Nanotechnologie, an Hersteller und Anwender, Wissenschaftler, Forscher, Förderer, Kapitalgeber und weitere Interessenten. Die Konferenzsprache ist Deutsch. Weitere Informationen zur Konferenz sind über www.nanoDE.de abrufbar.

nanoDE 2006

The screenshot shows a web browser window with the address <http://www.bmbf.de/de/684.php>. The page title is "BMBF: NanoFab - neue Wege in der Nanoelektronik". The header includes the BMBF logo and the text "Bundesministerium für Bildung und Forschung". A navigation bar at the top right contains links: Home | Kontakt | English | Sitemap | Impressum | Suche | Warenkorb. A large orange banner with the text "Ideen zünden!" is positioned below the header. The left sidebar contains a vertical menu with the following items: HIGHTECH-STRATEGIE, BILDUNG, FORSCHUNG, WISSENSCHAFT, INTERNATIONALES, MINISTERIUM, PRESSE, SERVICE, and BÜRGERTELEFON. Below the menu is a search box labeled "VOLLTEXTSUCHE" with the placeholder text "Suchbegriff eingeben" and a search button. The main content area features a section titled "HIGHTECH-STRATEGIE" with a sub-header "NanoFab - neue Wege in der Nanoelektronik". The text in this section describes the research funding and the establishment of the AMD-Chipfabrik and the FhG-Forschungszentrum für Nanoelektronische Technologien (CNT) in Dresden. The right sidebar contains a section titled "DOKUMENTE" with two entries: "Dresden wird zum wichtigsten Standort der europäischen Forschung für die Nanoelektronik" and "Unterzeichnung des Memorandum of Understanding". Below this is a section titled "PUBLIKATIONEN" with the sub-header "Nanotechnologie".

BMBF: NanoFab - neue Wege in der Nanoelektronik

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Bundesministerium für Bildung und Forschung

Ideen zünden!

HIGHTECH-STRATEGIE

BILDUNG

FORSCHUNG

WISSENSCHAFT

INTERNATIONALES

MINISTERIUM

PRESSE

SERVICE

BÜRGERTELEFON

VOLLTEXTSUCHE

Suchbegriff eingeben

HIGHTECH-STRATEGIE

NanoFab - neue Wege in der Nanoelektronik

Forschungsförderung schafft Arbeitsplätze. Das zeigt die Eröffnung der AMD-Chipfabrik für moderne Athlon-Prozessoren im Oktober 2005 und die Gründung des FhG-Forschungszentrums für Nanoelektronische Technologien (CNT) im Mai 2005 in Dresden sowie die Produktion von 300-mm-Wafern für die Chipherstellung in Freiberg. Dresden ist heute dank staatlicher Fördermittel Europas bedeutendster Standort für Mikro- und Nanoelektronik: Die Förderung dieser Technologien hat allein in der Region Dresden bereits 20.000 neue Arbeitsplätze geschaffen. Mit NanoFab fördert das BMBF neue Wege zur Fabrikation von Nanoelektronik.

DOKUMENTE

Dresden wird zum wichtigsten Standort der europäischen Forschung für die Nanoelektronik [PDF - 40,7 kB]

Gemeinsame Pressemitteilung der Partner zur Unterzeichnung des "Memorandum of Understanding"

Unterzeichnung des Memorandum of Understanding [PDF - 187,4 kB]

Rede der Bundesministerin für Bildung und Forschung Edelgard Bulmahn anlässlich der Unterzeichnung des Memorandums of Understanding für die Fraunhofer-Einrichtung "Center of Nanoelektronik Technologies FhG-CNT" am 30. August 2004 in Dresden.

PUBLIKATIONEN

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