Overview of Simulation Strategies for Nanoelectronics

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Outline

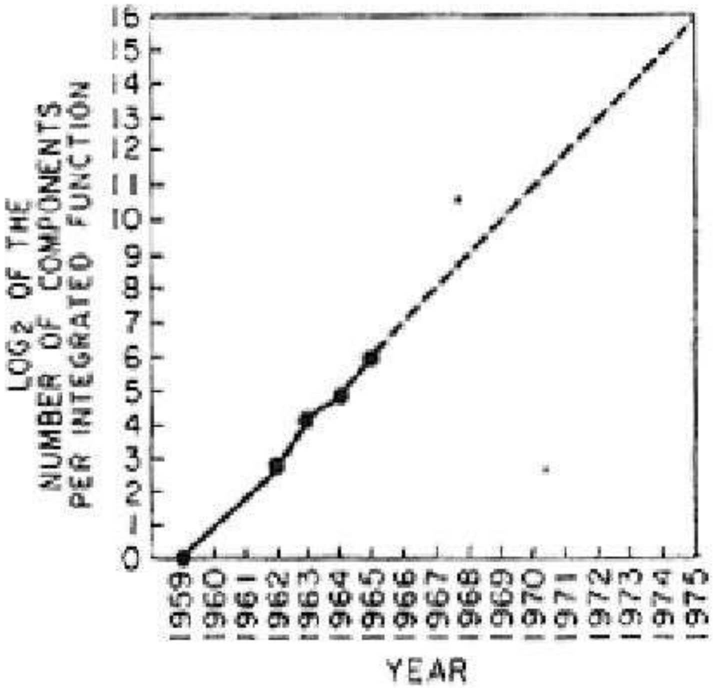
- ⇒ **Introduction to Nanoelectronics**
- ⇒ **Nanoelectronics in ITRS**
- ⇒ **Molecular Simulation**
- ⇒ **Conclusion**

Moore’s Law

Gordon E. Moore, 1965

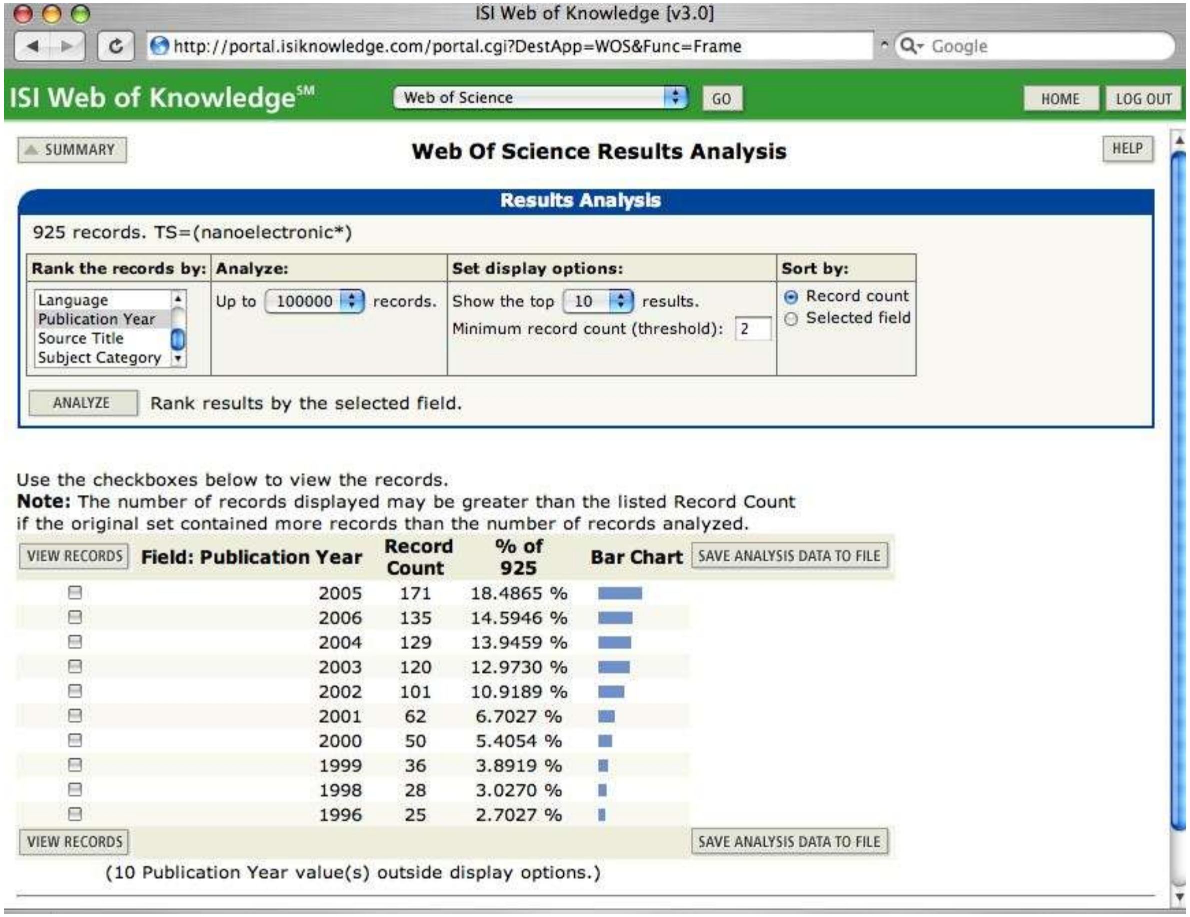
Cramming more components onto integrated circuits

- ⇒ **Exponential growth.**
- ⇒ **Cost per function reduction:**
  - → 25-29% per year.
- ⇒ **Market growth:**
  - → On average 17% per year.
- ⇒ **The law holds for about 45 years.**
- ⇒ **ITRS**
  - → Industry want to keep with this law further.



Papers on Nanoelectronics: Web of Science

- ⇒ **925 papers:**
  - → Refereed journals.
- ⇒ **Search includes:**
  - → Title,
  - → Keywords,
  - → Abstract.



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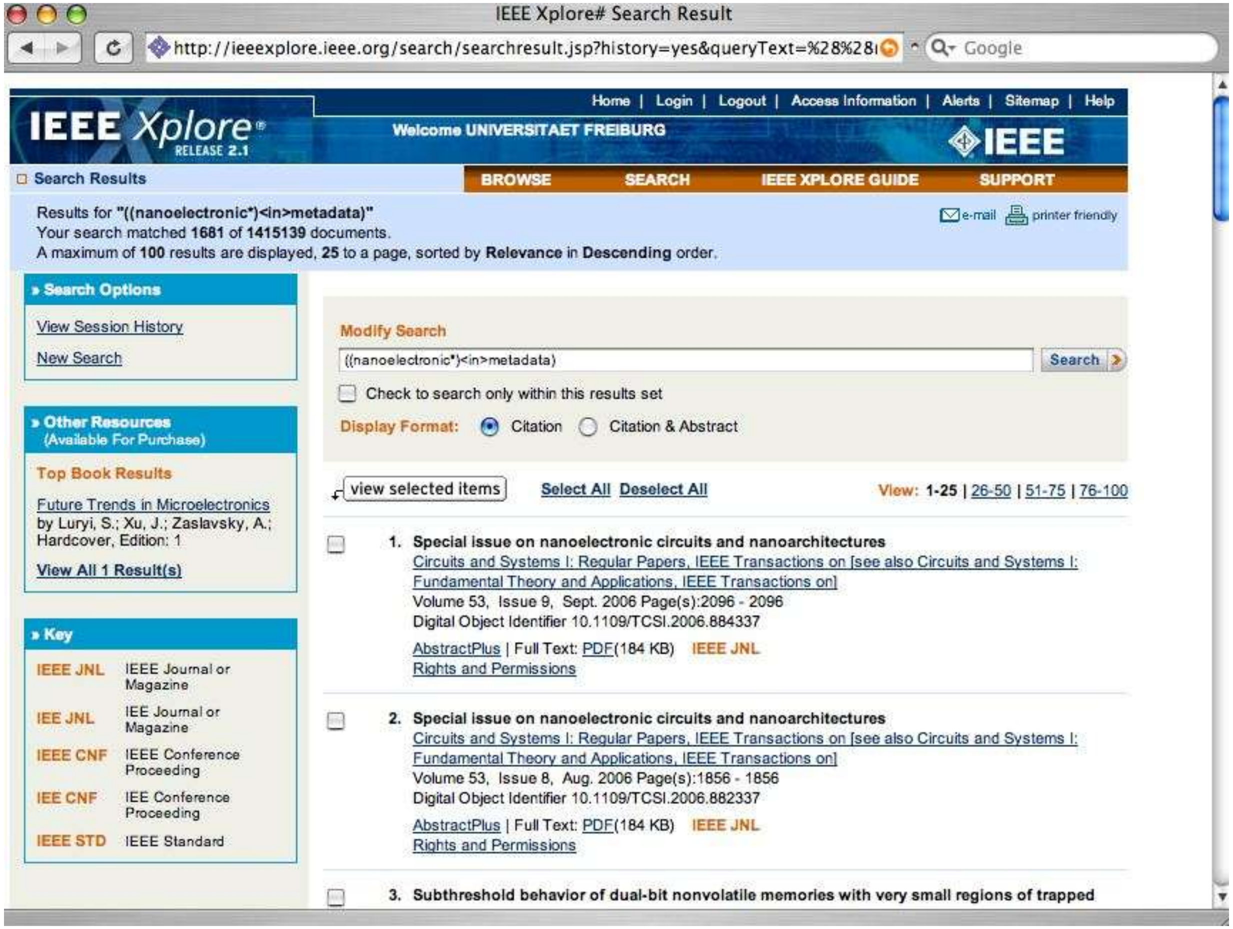
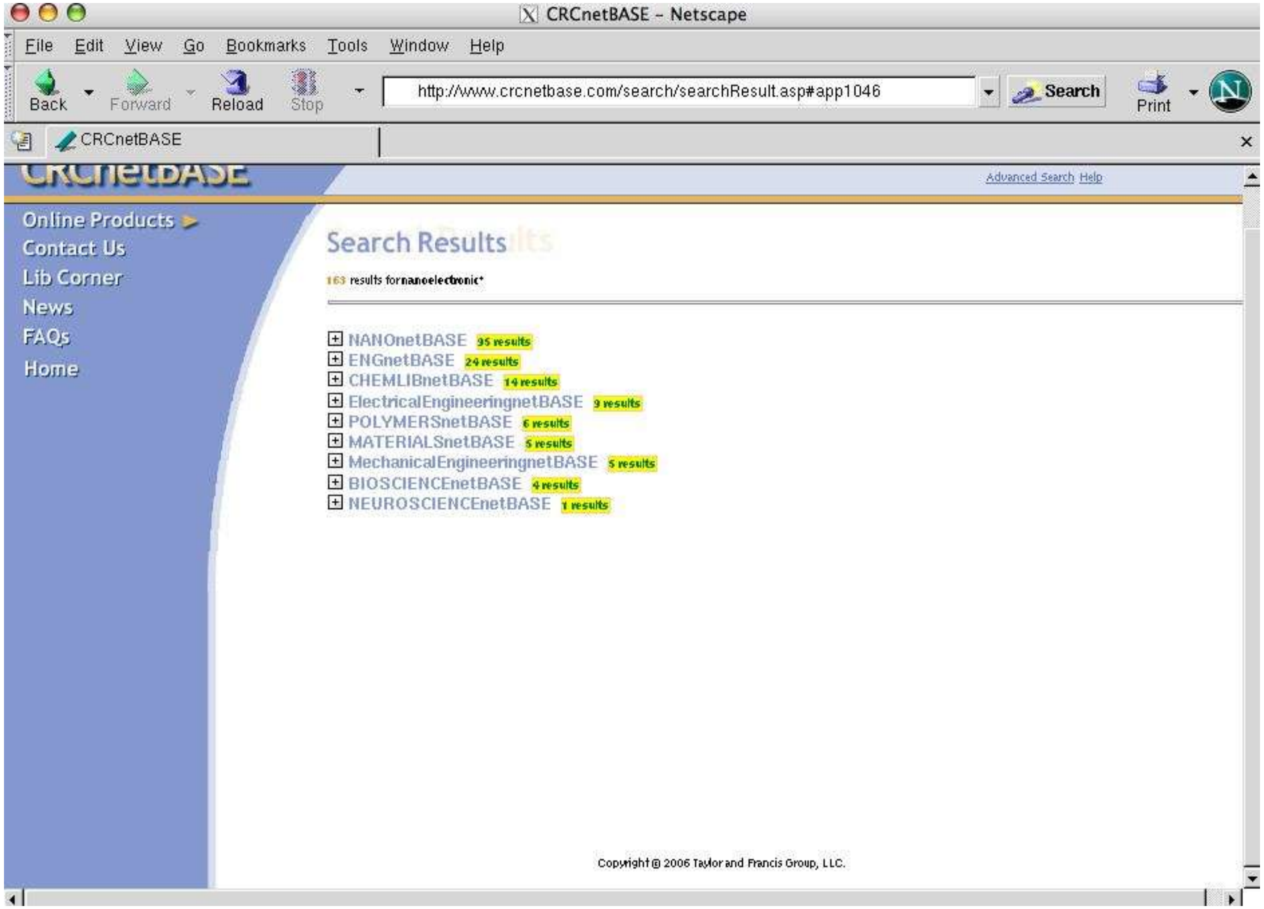
Papers on Nanoelectronis: IEEE

- ⇒ 1681 papers.
- ⇒ Only IEEE publications.
- ⇒ IEEE conferences are included.



CRC On-Line Book Chapters

⇒ **163 Hits**



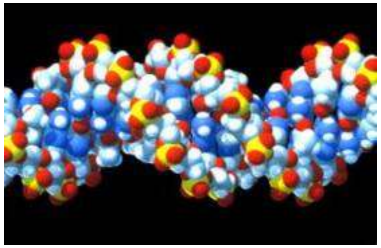
What is Nanoelectronics?

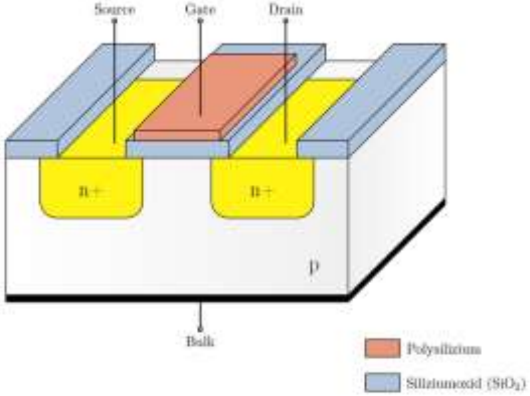
⇒ **Electronics on a nanometer scale (feature size less than 100 nm)**

⇒ **Si-based (CMOS) and beyond-CMOS**

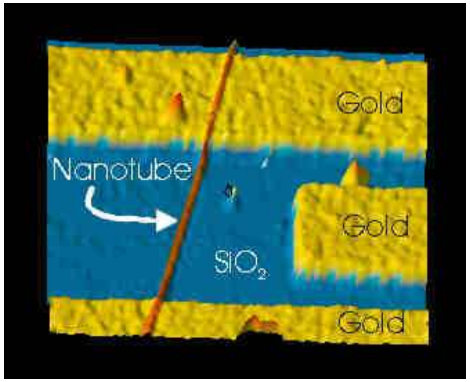
⇒ **Is “electro” important?**

→ Information processing



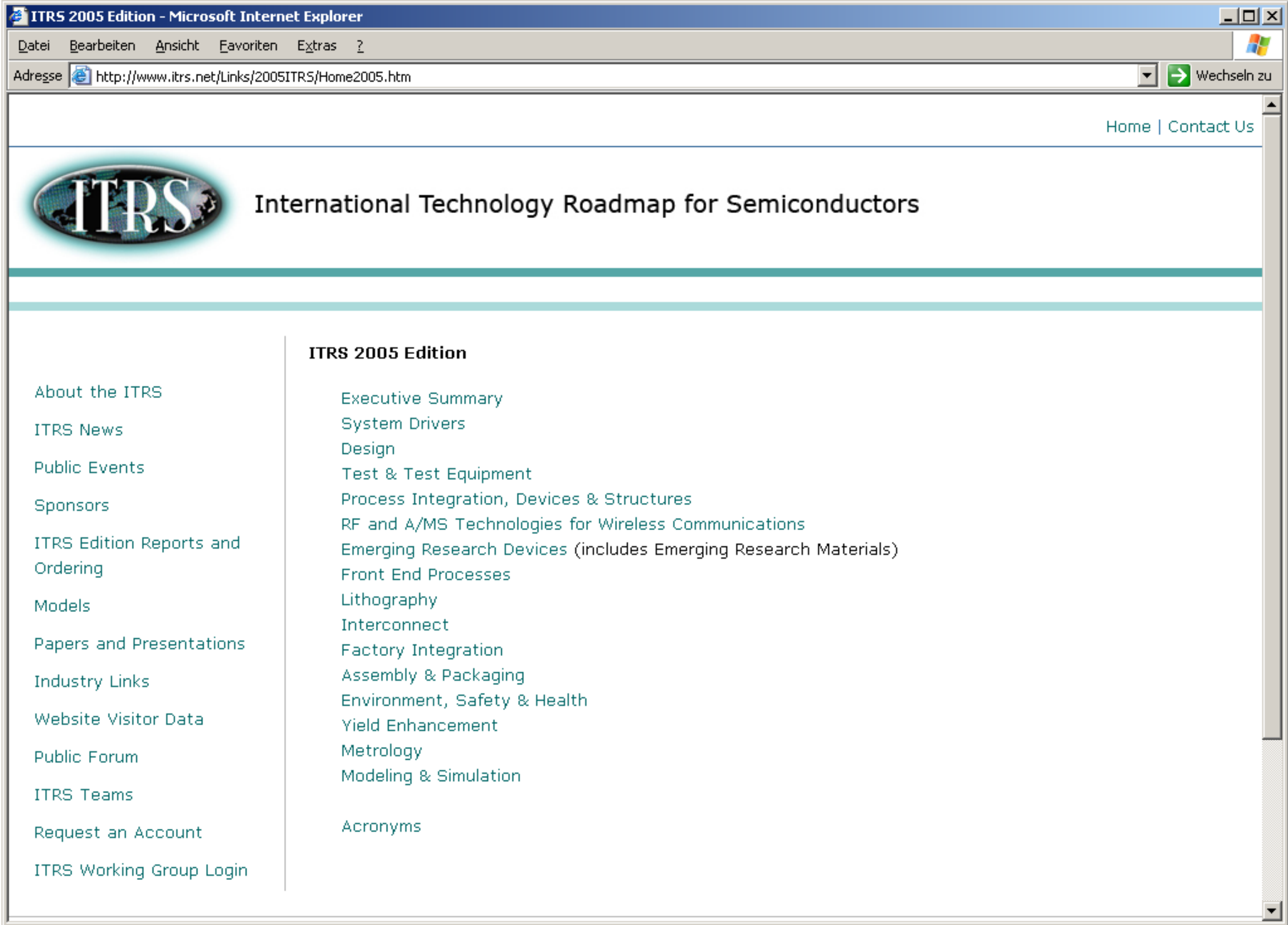


Carbon nanotube transistor



ITRS 2005

What technical capabilities need to be developed for the industry to stay on Moore's Law and the other trends?



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Contributors

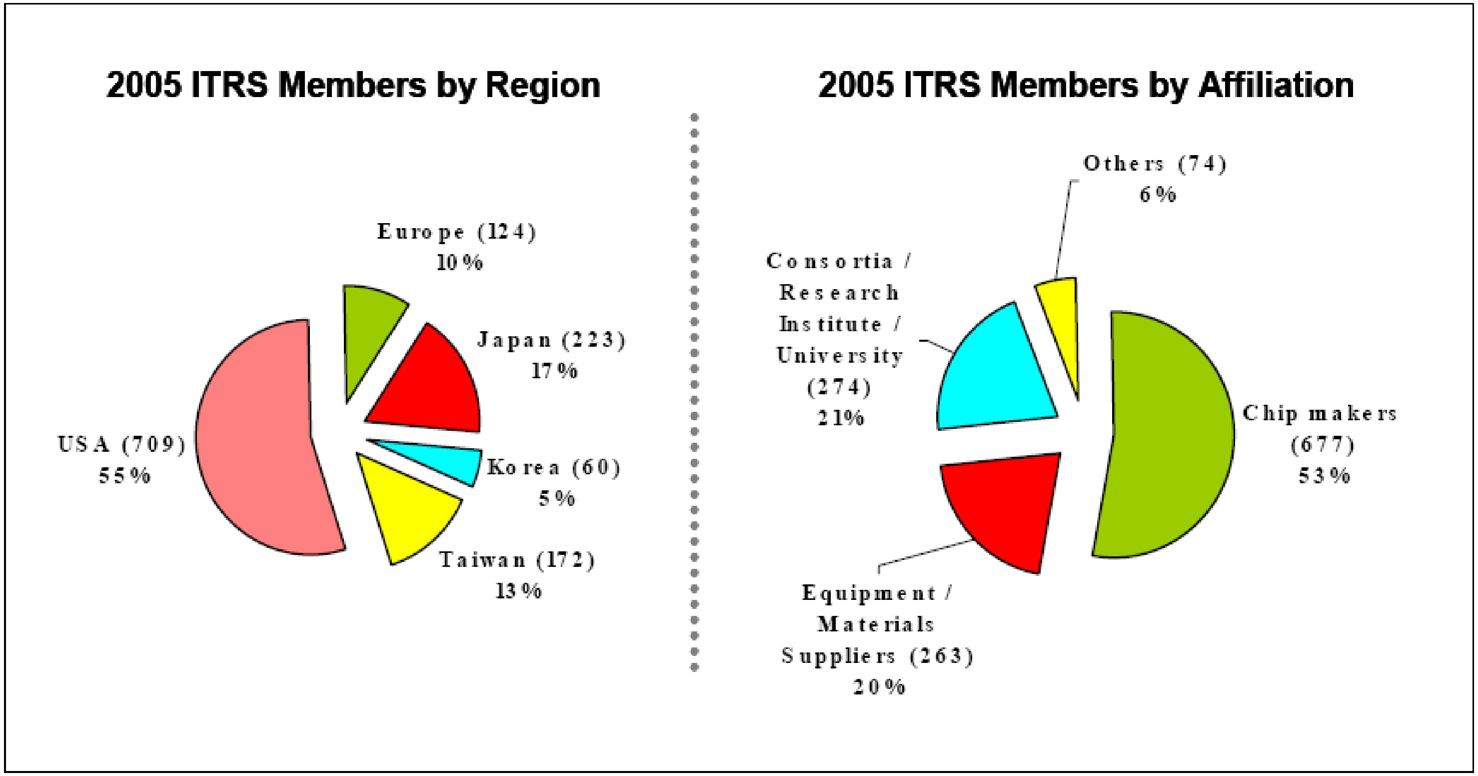


Figure 1 Composition of the ITRS Teams—1288 Global Participants

Structure

⇒ **Executive Summary (89 pages)**

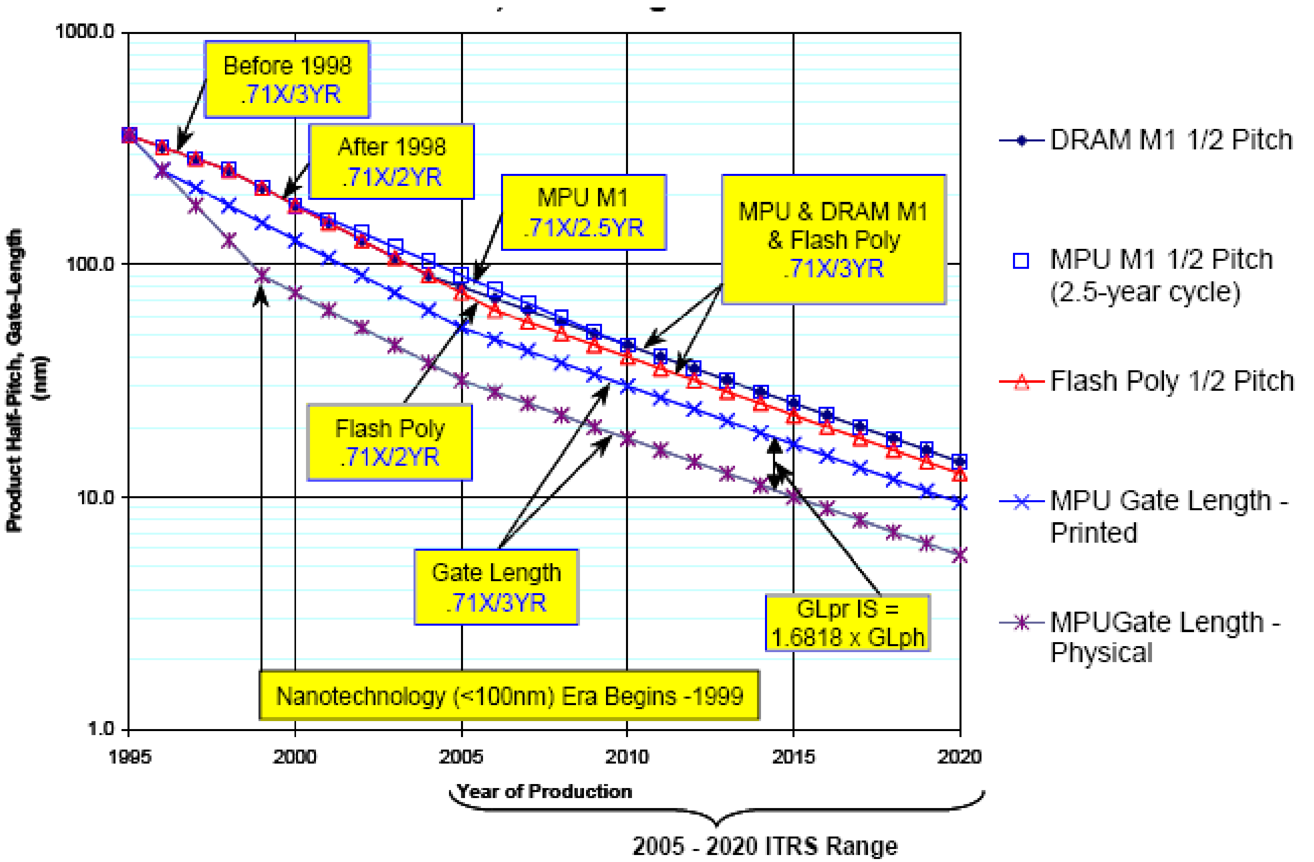
⇒ **11 Focus International Technology Working Groups**

- → …
- → Emerging Research Devices / Emerging Research Materials
- → …

⇒ **4 Crosscut International Technology Working Groups**

- → …
- → Modeling and Simulation

ITRS Product Technology Trend



Near-term Years:
2005 to 2013

Long-term Years:
2014 to 2020

Scaling CMOS

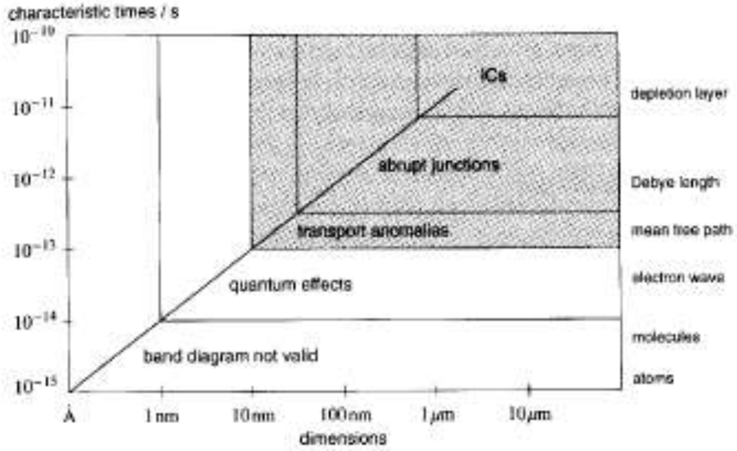
Table 76a Lithography Technology Requirements—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
DRAM and Flash									
DRAM ½ pitch (nm)	80	70	65	57	50	45	40	35	32
Flash ½ pitch (nm) (un-contacted poly)	76	64	57	51	45	40	36	32	28
Contact in resist (nm)	94	79	70	63	56	50	44	39	35
Contact after etch (nm)	85	72	64	57	51	45	40	36	32
Overlay [A] (3 sigma) (nm)	15	13	11	10	9	8	7.1	6.4	5.7
CD control (3 sigma) (nm) [B]	8.8	7.4	6.6	5.9	5.3	4.7	4.2	3.7	3.3

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

CMOS and beyond CMOS

- ⇒ CMOS is the workhorse of the industry.
- ⇒ Yet, scaling of CMOS has technological and physical limits.
- ⇒ The semiconductor industry's future success continues to depend on new ideas.
- ⇒ Chapter on Emerging Research Devices including Emerging Research Materials.



Goser Gloeserkoetter Dienstuhl

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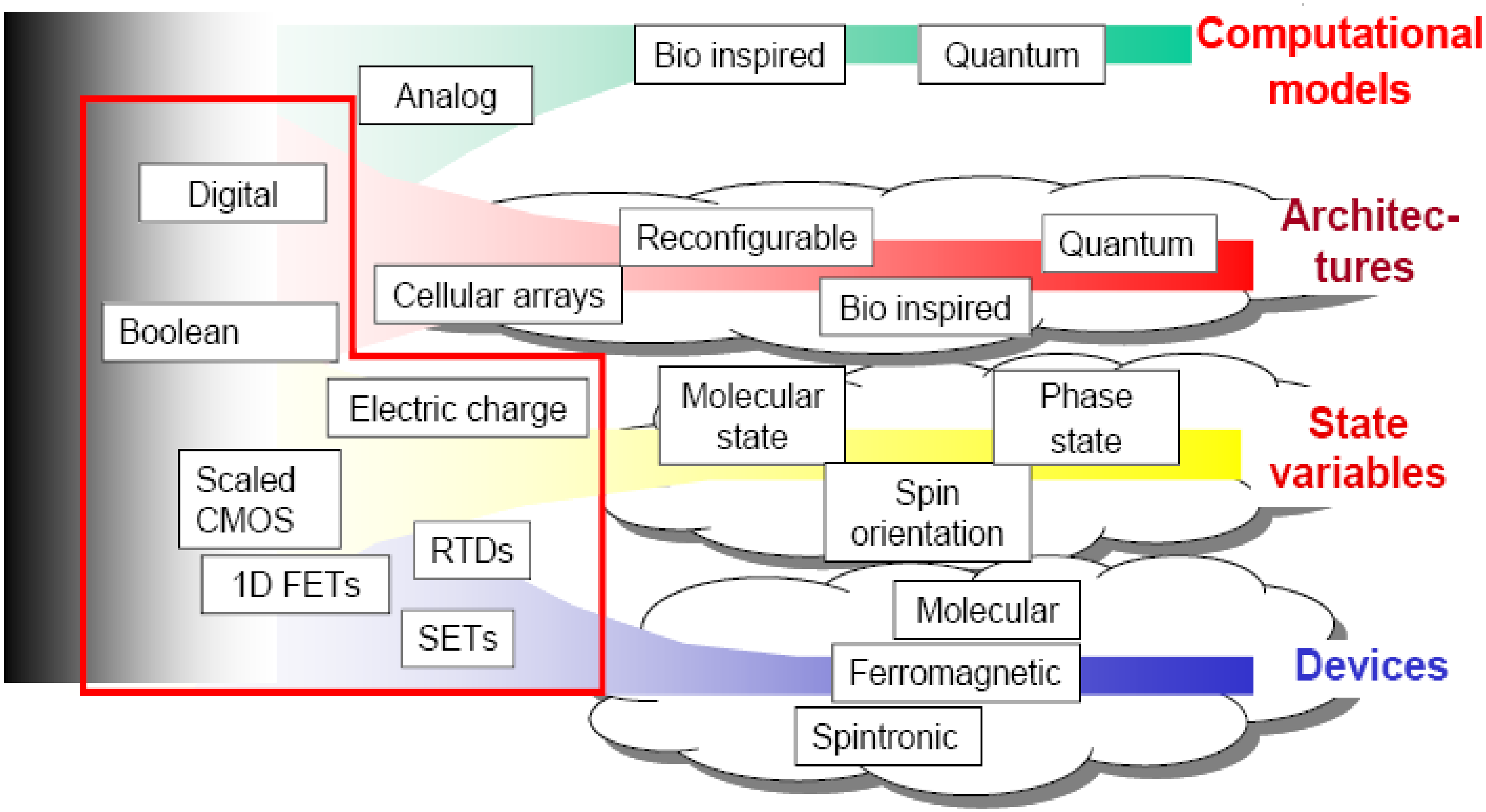
Taxonomy for Nano Information Processing



Devices and Architectures

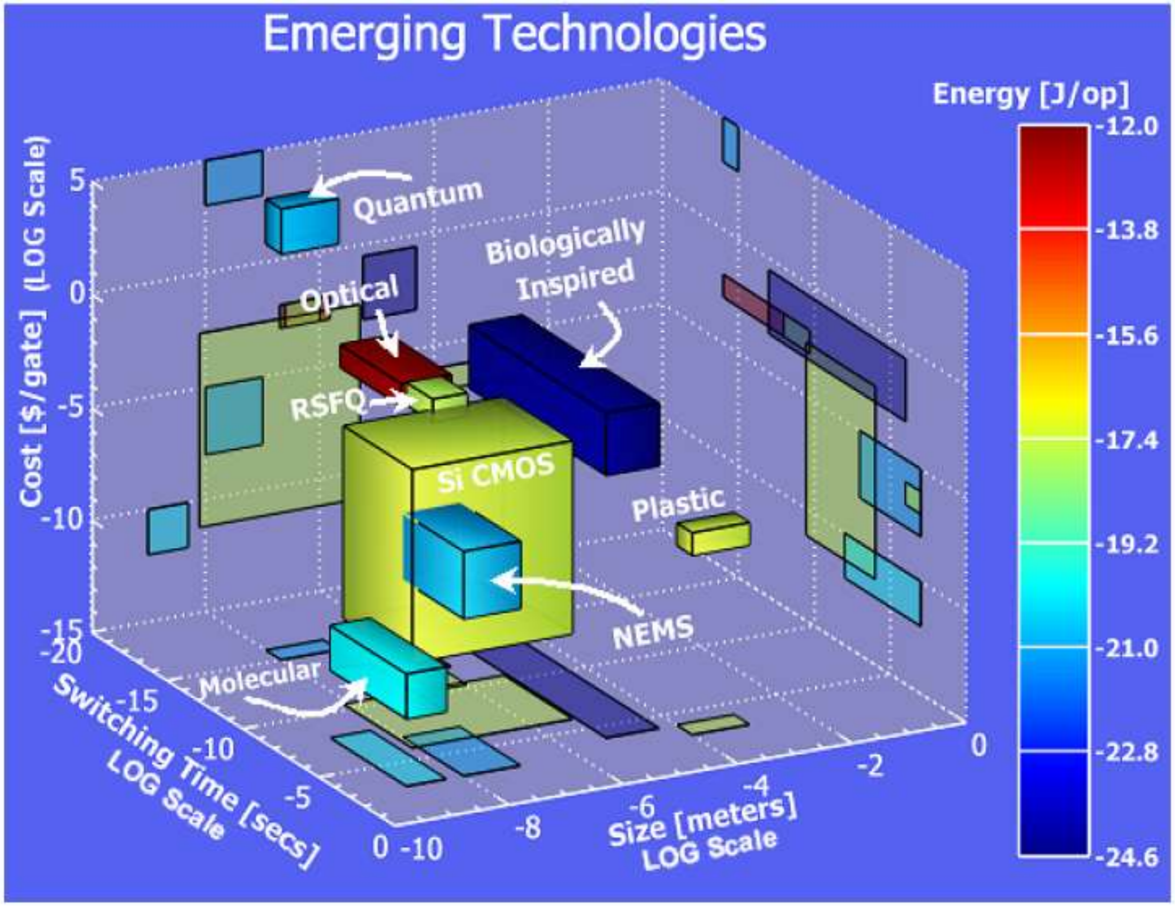
⇒ **Devices:**

- → Carbon nanotube and nanowires,
- → Ferroelectric FET memory,
- → Molecular,
- → Nano floating gate memory,
- → Polymer memory,
- → Polymer transistor,
- → Resonant tunneling devices,
- → Spin transistor.

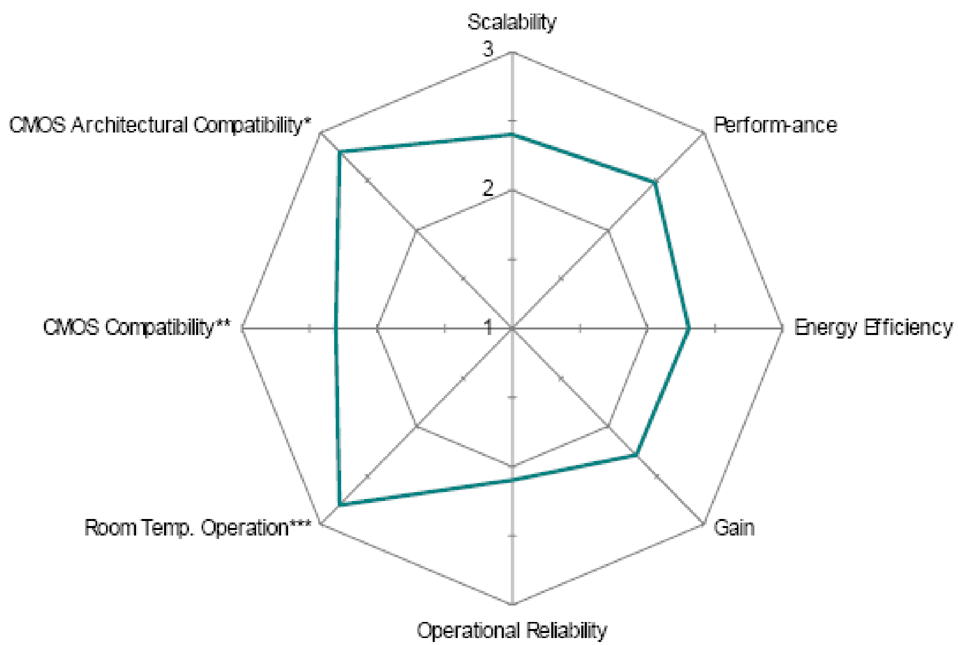
⇒ **Architectures:**

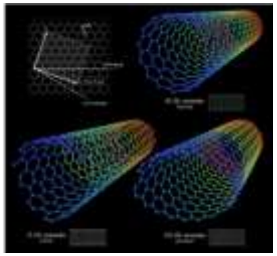
- → Quantum Cellular Automata,
- → Cellular Nonlinear Networks,
- → Reconfigurable Implementations,
- → Biologically Inspired Implementation.

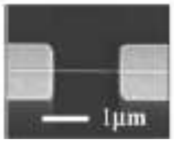
Emerging Technologies and CMOS



Potential Solutions for Logic Devices (CNT and NW)





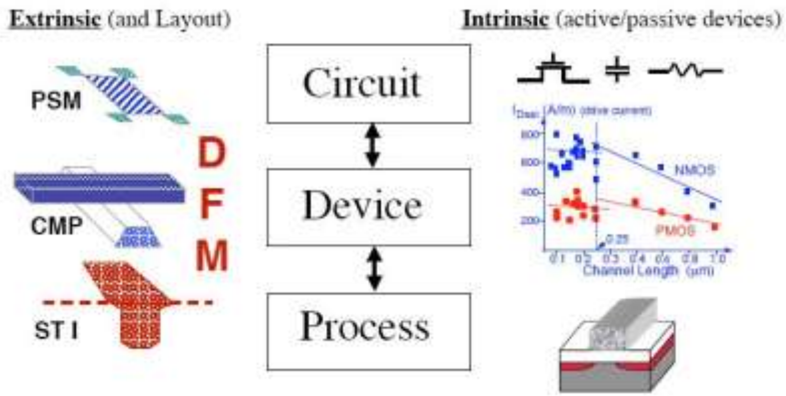


NW-FET

3	Substantially exceeds CMOS * *or* is compatible with CMOS architecture ** *or* is monolithically integrable with CMOS wafer technology ****or* is compatible with CMOS operating temperature (i.e., **Substantially Better than Silicon Logic**)
2	Comparable to CMOS * *or* can be integrated with CMOS architecture with some difficulty ** *or* is functionally integrable (easily) with CMOS wafer technology ****or* requires a modest cooling technology, $T \geq 77K$ (i.e., **Comparable to Silicon Logic**)
1	Substantially (2×) inferior to CMOS * *or* can not be integrated with CMOS architecture ** *or* is not integrable with CMOS wafer technology ****or* requires very aggressive cooling technology, $T < 77K$ (i.e., **Substantially Worse that Silicon Logic**)

Modeling and Simulation: Technology CAD for CMOS

- ⇒ **High-frequency device and circuit modeling**
- ⇒ **Front-end process modeling**
- ⇒ **Integrated modeling of equipment and materials**
- ⇒ **Lithography simulation**
- ⇒ **Thermo-mechanical-electrical modeling for interconnections and packages**



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Modeling and Simulation: Molecular Simulation

⇒ **Ultimate nanoscale CMOS simulation**

⇒ **Nano-scale modeling of novel devices**

⇒ **Modeling of new materials**

⇒ **Nanoscale simulation capability including accurate atomistic and quantum effects**

⇒ **Algorithms:**

- → Efficient atomistic/quantum models; ab-initio or molecular dynamics based topography simulations;
- → Multi-scale simulation (atomistic-continuum); fast coupling of equipment-topography-electrical-reliability models; hierarchichal full-chip simulation.

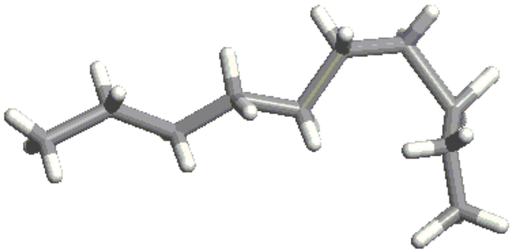
Model Order Reduction for EDA

⇒ **Current EU projects:**

- → COMSON (**CO**upled **M**ultiscale **S**imulation and **O**ptimization in **N**anoelectronics) http://www.comson.org/
- → CHAMELEON RF, (**C**omprehensive **H**igh-**A**ccuracy **M**odelling of **EL**ectromagnetic **E**ffects in C**o**mplete **N**anoscale **RF** blocks) http://www.chameleon-rf.org/
- → O-MOORE-NICE, (**O**perational **MO**del **O**rder **RE**duction for **N**anoscale **IC** **E**lectronics)

Course: Molecular Simulation for MST

- ⇒ **J. G. Korvink, E. B. Rudnyi**
  - → http://evgenii.rudnyi.ru/teaching.html#md
- ⇒ **Introductory course for MST engir**
- ⇒ **12 lectures, 3 computational labs**



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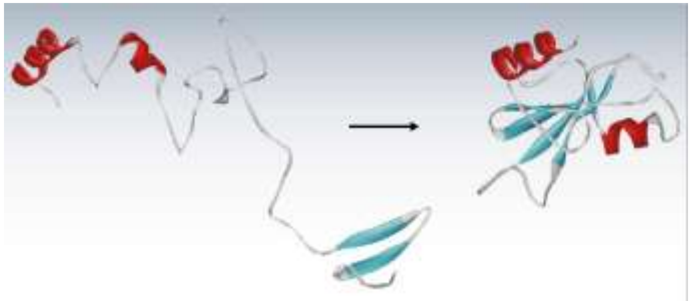
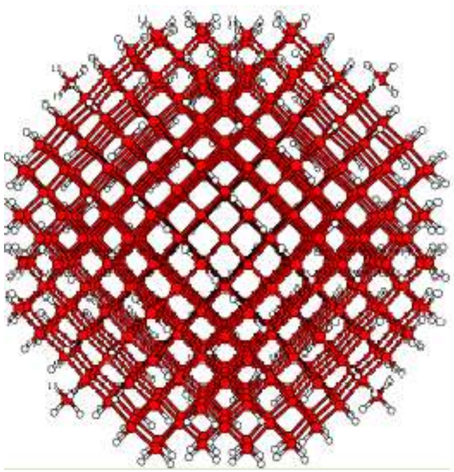
From the First Principles



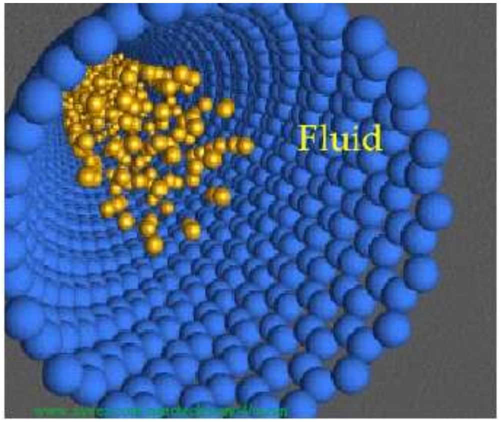
- ⇒ **Ab initio (*from the beginning*)**
- ⇒ **Input: A few fundamental constants**
  - → electron mass, proton mass, Plank constant, speed of light, …
- ⇒ **Output: Everything**
- ⇒ **Computationally expensive**
- ⇒ **Blue Gene: IBM Petaflop computer**
  - → Protein folding

Hierarchy

⇒ **Potential Energy Surface (0 K)**
- → Electronic Schrödinder Equation
- → Semiempirical methods
- → Molecular Mechanics



⇒ **Adding Entropy and Temperature**
- → Molecular Dynamics
- → Monte Carlo



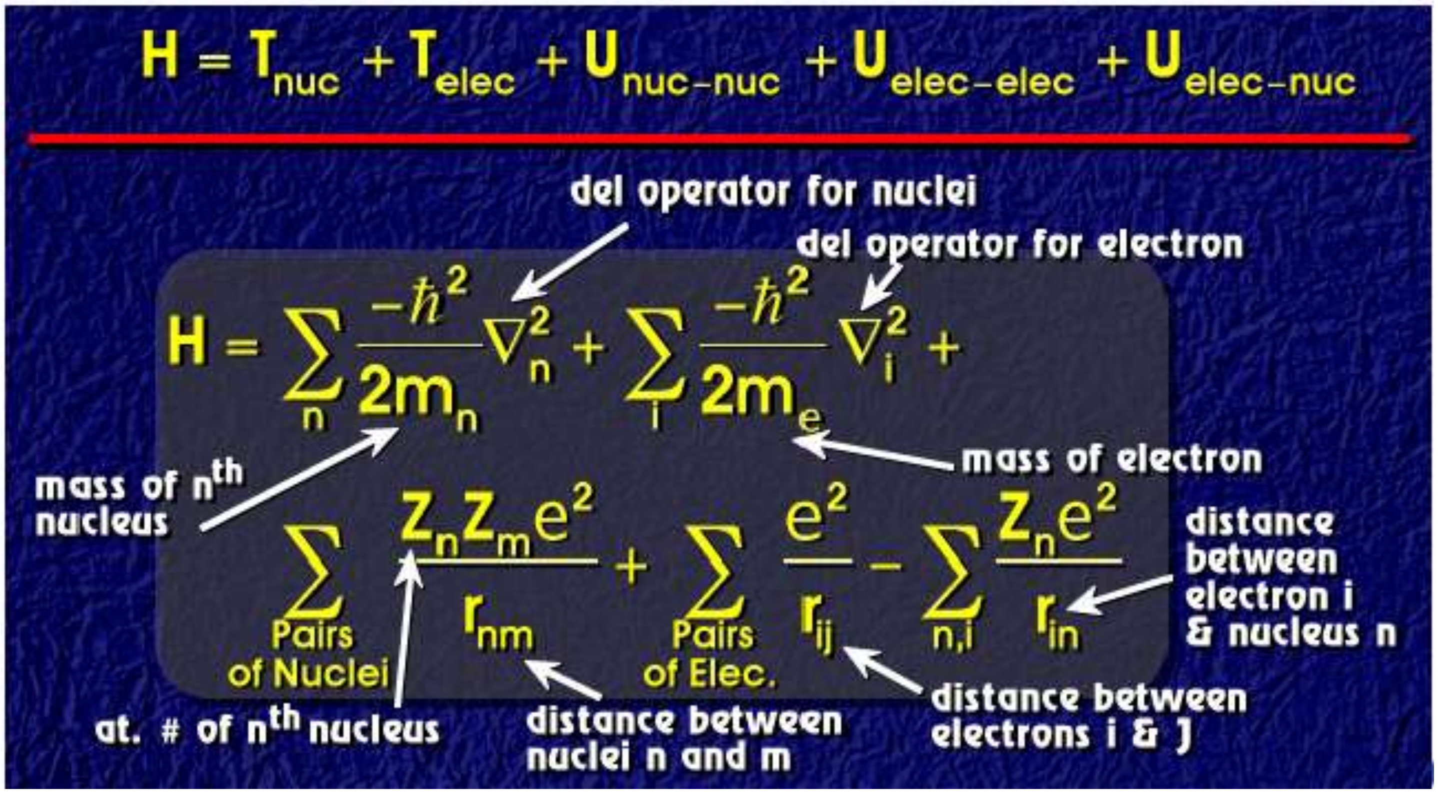
⇒ **QSAR (empirical correlations)**

Schrödinger Equation

Nuclei ($\boldsymbol{R}$) and electrons ($\boldsymbol{r}$) :

$\Psi(\boldsymbol{R}, \boldsymbol{r})$

$$H\psi = E\psi$$



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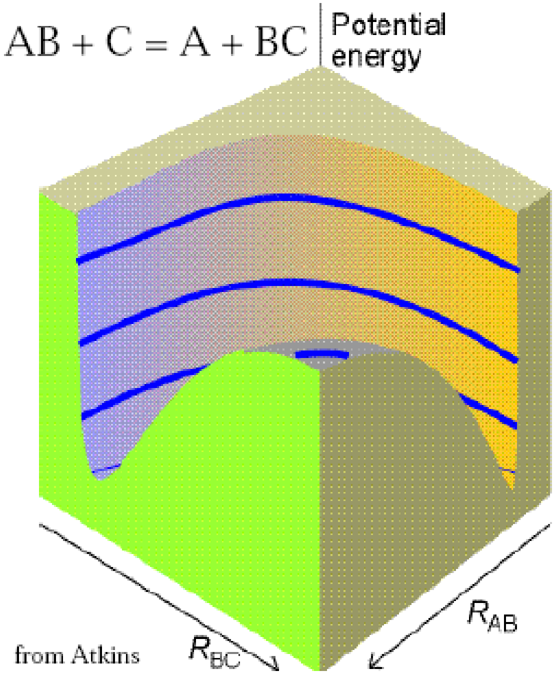
Potential Energy Surface

- ⇒ **Born-Oppenheimer Approximation**
- ⇒ Proton is 1836 times heavier than electron.
  - → **Factorize for nuclei part**

$$\Psi(\boldsymbol{R}, \boldsymbol{r}) = \Psi(\boldsymbol{R})\psi(\boldsymbol{r};\boldsymbol{R})$$

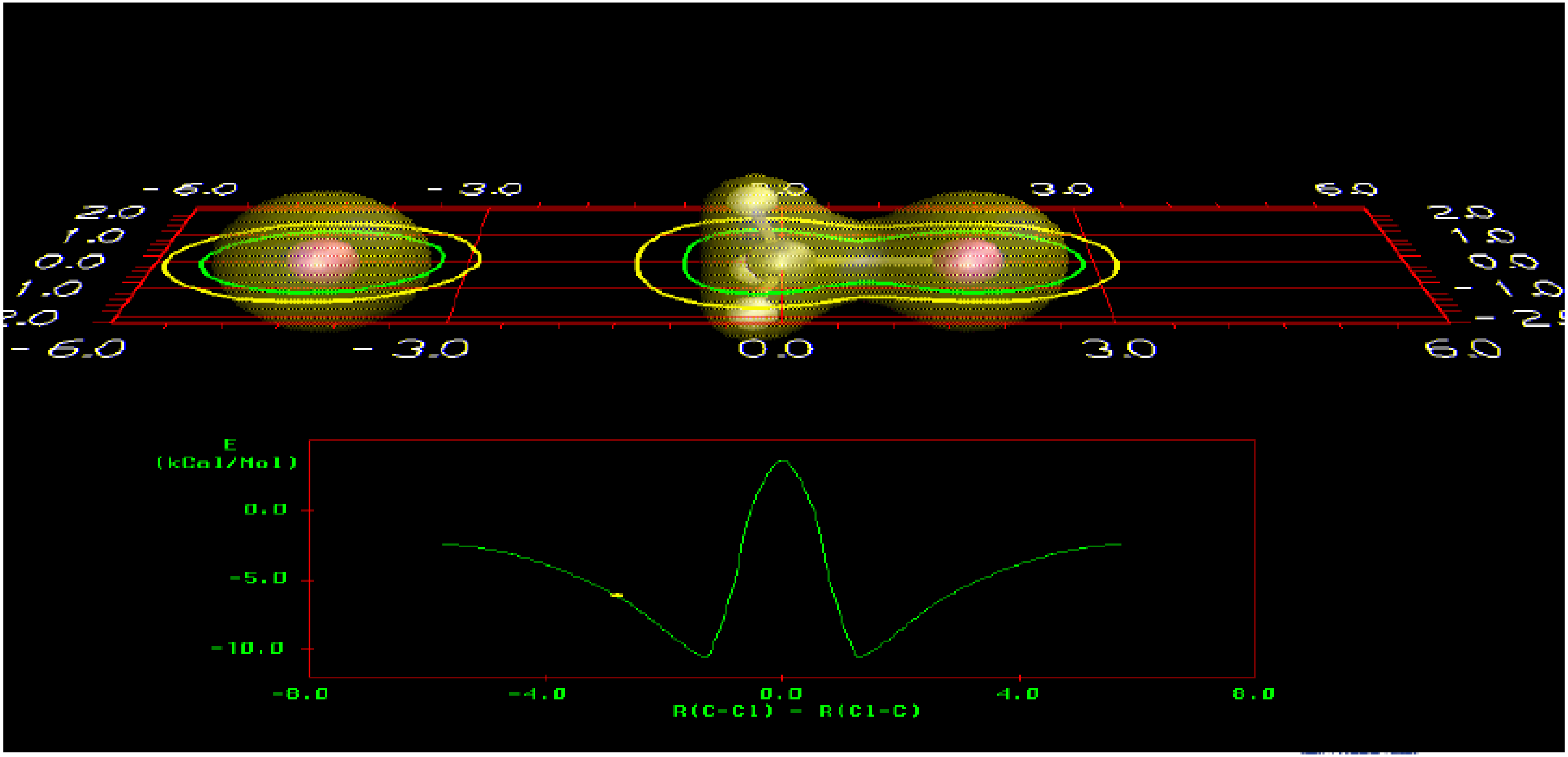
  - → **Schrödinger equation for electrons**

$$H_{el}\psi(\boldsymbol{r};\boldsymbol{R}) = E_{el}(\boldsymbol{R})\psi(\boldsymbol{r};\boldsymbol{R})$$

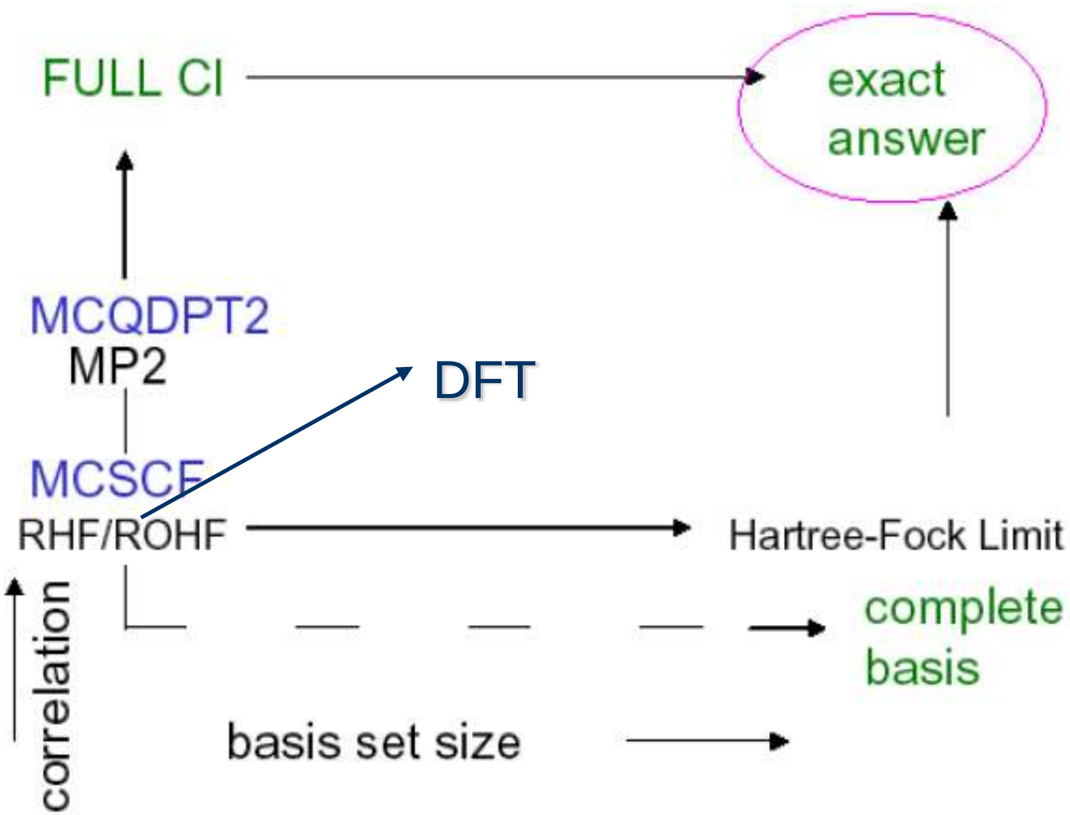


PES Example

scsg9.unige.ch/fln/eng/toc.html



Quantum Chemistry Methods



Molecular orbitals

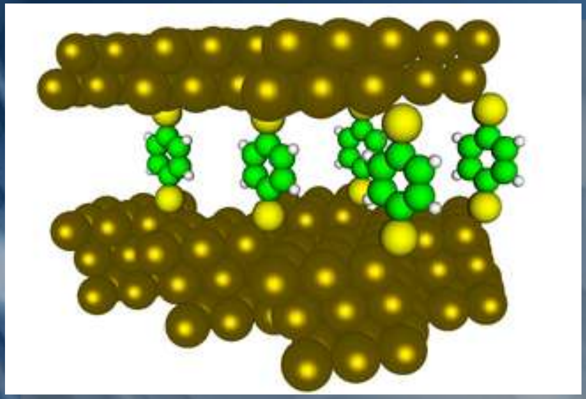
$$\Psi(1,2,\ldots,N) \approx \psi(1)\psi(2)\ldots\psi(N)$$

Atomic orbitals

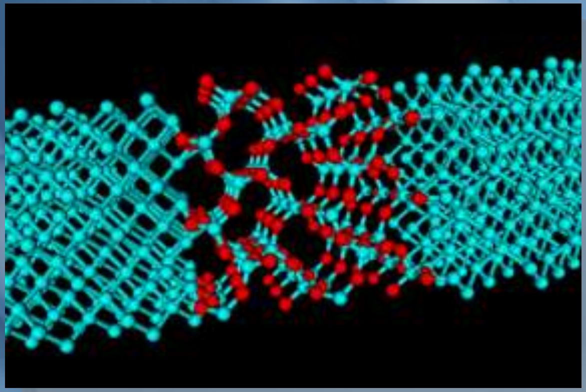
$$\psi = \sum_i c_i \vartheta_i$$

What kind of software is needed?

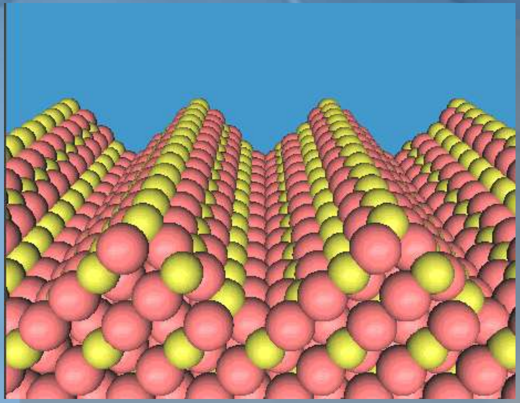
As the main challenge in nanoscale technology derive from quantum phenomena across nanoscale junctions, interfaces and surfaces, it is critical to be able to accurately model such phenomena from quantum theory



Junctions



Interfaces



Surfaces

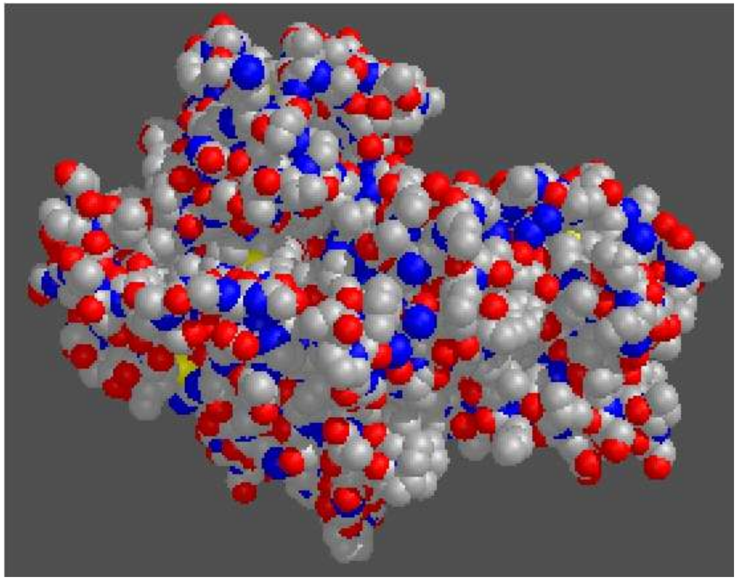
Semiempirical Methods

⇒ **Consider valence electrons only**

⇒ **Neglect some integrals**

⇒ **Parameterize the others**

⇒ **Accuracy depends on the parameterization**

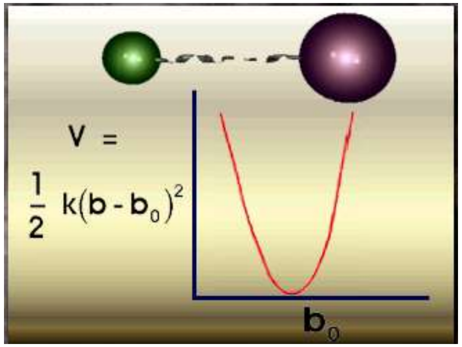


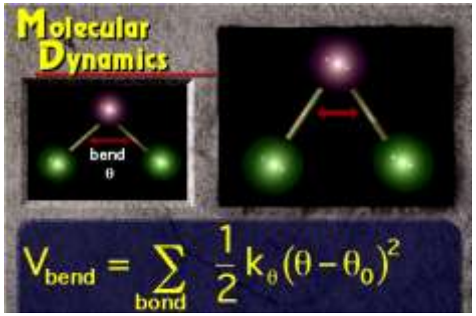
Molecular Mechanics

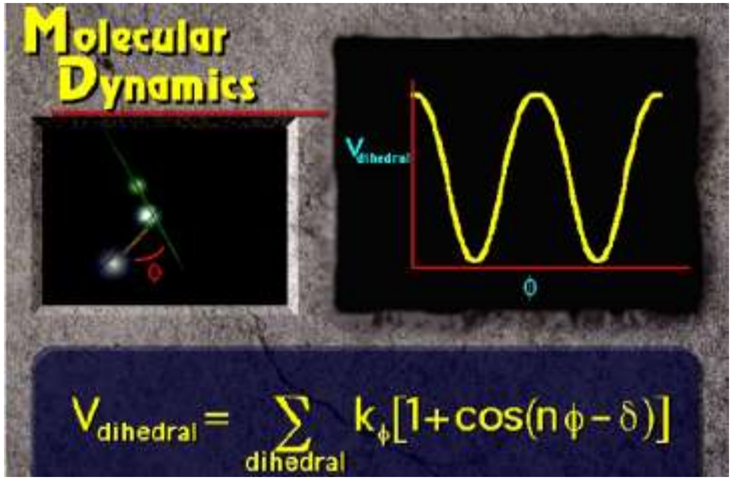
⇒ **Empirical force field**

- → Bonding: streching, bending, torsion, cross-terms;
- → Not-bonding: van der Vaals, electrostatic, hydrogen, etc...

⇒ **Accuracy depends on the force field employed**

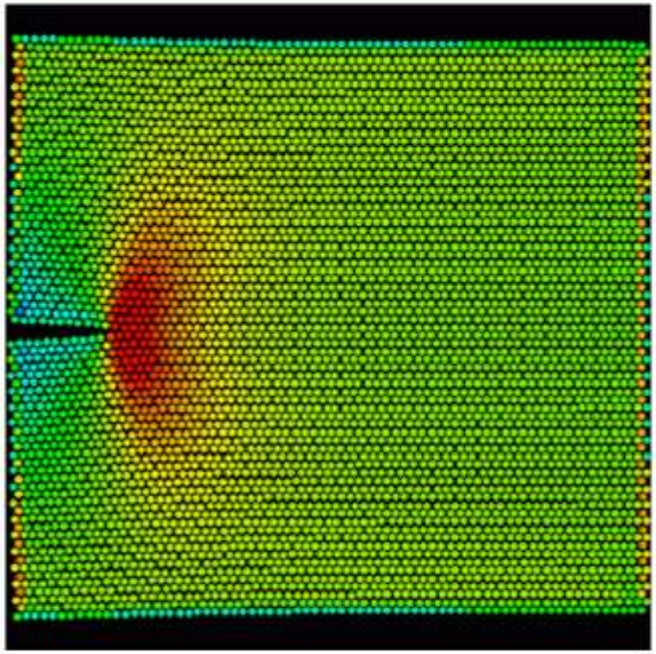






Molecular Dynamics and Monte Carlo

- ⇒ **Input:**
  - → Potential energy surface
- ⇒ **Output:**
  - → Heat conductivity, viscosity, …
- ⇒ **Time average**
  - → Integrating in time
- ⇒ **Ensemble average**
  - → Sampling according to Bolztmann distribution



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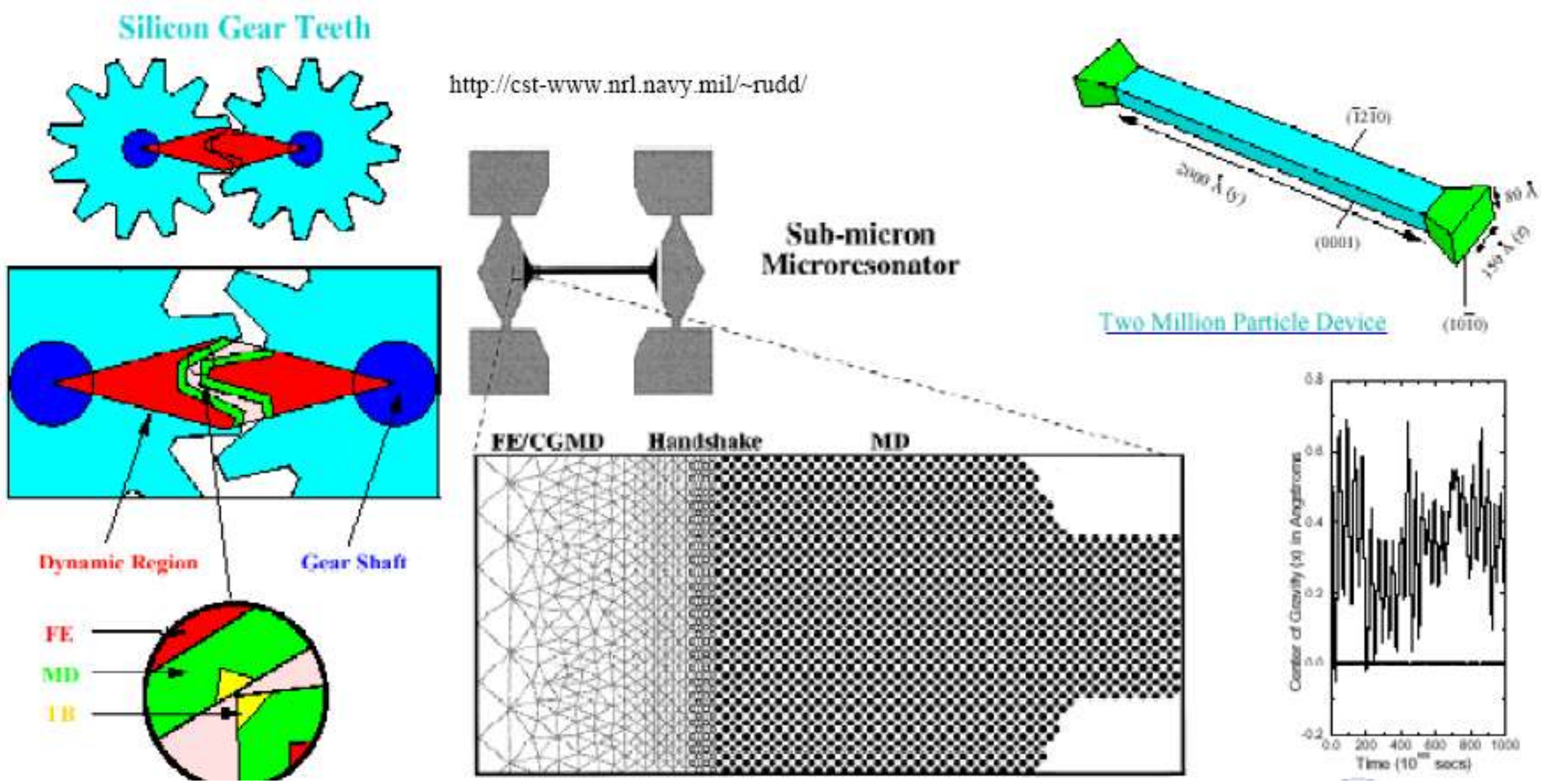
Multiscale Simulation



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Conclusion

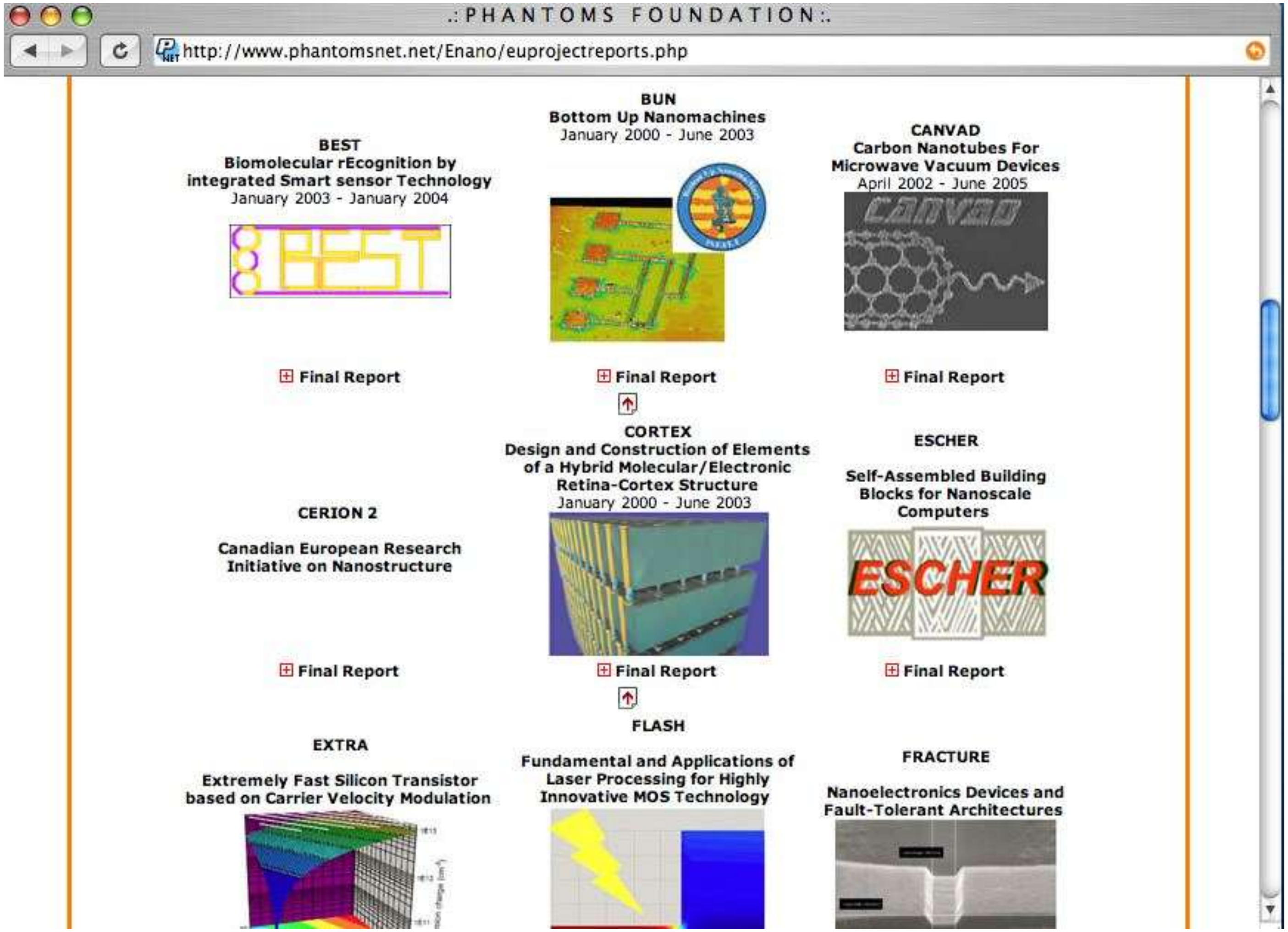
⇒ **Beyond CMOS: New ideas for nanoelectronics**

⇒ **Molecular simulation is a natural way to check new ideas**

⇒ **Tight collaboration between industry and academia**

Nanoelectronics

EU projects



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niac
European Nanoelectronics Initiative Advisory Council
ENIAC is the European Technology Platform for Nanoelectronics
The principal mission of ENIAC is to:
Provide a strategic research agenda for the nanoelectronics sector, with respect to R&D
Set out strategies and roadmaps to achieve this vision through the Strategic Research Agenda and other associated documents;
Stimulate increased and more effective and coherent public and private investment in R&D in the nanoelectronics sector;
Contribute to improving convergence between EC, national, regional and private R&D actions on nanoelectronics within the European Research Area Framework;
Enhance networking and clustering of the R&D capacity in Europe;
Promote European commitment to R&D thus ensuring Europe as an attractive location for researchers;
Interact with other policies and actors at all levels that influence the competitiveness of the sector such as education and training, competition, IPR, finance and investment, etc.
ENIAC Highlights
ENIAC Strategic Research Agenda (full version) (PDF)
Forum of Stakeholders 23 November 2005
Forum of Stakeholders - How to express interest (PDF)
First meeting of ENIAC Forum of Stakeholders
Strategic Research Agenda - presentation (PDF)
Strategic Research Agenda - executive summary (PDF)
21 December 2004 - the first meeting of the Steering Committee
The 2020 Vision document (PDF)
Nanoelectronics Technology Platform - overview document (PDF)
How to express your interest
You are invited to submit an Expression of Interest that should include a short overview of the organisation's activities in the nanoelectronics sector as well as the motivation for participating in ENIAC. A short CV of the person from the organisation that would be the contact point (including a web link) should also be included.

BMBF Nanotechnology

BMBF Nanoelectronics